SiFive FE310-G002 PreliminaryDatasheet

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Release Information

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>v1p0</td>
<td>April 12, 2019</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
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Chapter 1

FE310-G002 Description

1.1 Features

• SiFive E31 Core Complex up to 320MHz.
• Flexible clocking options including internal PLL, free-running ring oscillator and external 16MHz crystal.
• 1.61 DMIPs/MHz, 2.73 Coremark/MHz
• RV32IMAC
• 8kB OTP Program Memory
• 8kB Mask ROM
• 16kB Instruction Cache
• 16kB Data SRAM
• 3 Independent PWM Controllers
• External RESET pin
• JTAG, SPI I2C, and UART interfaces.
• QSPI Flash interface.
• Requires 1.8V and 3.3V supplies.
• Hardware Multiply and Divide

1.2 Description

The FE310-G002 is the second Freedom E300 SoC. The FE310-G002 is built around the E31 Core Complex instantiated in the Freedom E300 platform.

The FE310-G002 Manual should be read together with this datasheet. This datasheet provides electrical specifications and an overview of the FE310-G002.

The FE310-G002 comes in a convenient, industry standard 6x6mm 48-lead QFN package (0.4mm pad pitch).
Chapter 2

FE310-G002 Pins

2.1 FE310-G002 Pinout

The FE310-G002 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) should be connected directly to the ground plane.
2.2 Pin Descriptions

2.3 Power Pins

VDD (6, 30, 46) : Core supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

IVDD (11, 32, 47) : I/O supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.

AON_VDD (23) : AON supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

AON_IVDD (19) : AON I/O supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

OTP_AIVDD (12) : OTP supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.

PLL_AVDD (7) : PLL supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.
PLL_AVSS (8) : Isolated PLL supply bypass. Connect through a 1uF ceramic capacitor to PLL_AVDD. This pin is not to be connected directly to GND.

GND (49) : Exposed paddle is a ground return and should be connected directly to the ground plane.

2.4 Crystal Drivers

XTAL_XI (9) : 16MHz Crystal Input
XTAL_XO (10) : 16MHz Crystal Output

An external 16MHz crystal may be connected between the two XTAL pins. The crystal should have a capacitive load of 12 pF and an ESR 80 Ohms. An external oscillator may also be used to drive the FE310-G002 through the XTAL_XI input, in which case the XTAL_XO pin should be left floating. The external oscillator should operate between GND and the 1.8V VDD supply.

2.5 JTAG

JTAG_TCK (13) : JTAG TCK Input
JTAG_TDO (14) : JTAG TDO Output
JTAG_TMS (15) : JTAG TMS Input
JTAG_TDI (16) : JTAG TDI Input

Please refer to the FE310-G002 Manual for information on the JTAG and debug facilities.

2.6 QSPI

QSPI_DQ_3 (1) : Bidirectional Quad SPI Data Line
QSPI_DQ_2 (2) : Bidirectional Quad SPI Data Line
QSPI_DQ_1 (3) : Bidirectional Quad SPI Data Line
QSPI_DQ_0 (4) : Bidirectional Quad SPI Data Line
QSPI_CS (5) : Quad SPI Chip Select OUTPUT, Active Low.
QSPI_SCK (48) : Quad SPI Clock OUTPUT

Please refer to the FE310-G002 Manual for information on the SPI FLASH interface and to the Applications Notes and Errata section of this datasheet for information in the SPI implementation.

2.7 GPIO Multiplexed Outputs

The General Purpose Input/Output pins are multiplexed with PWM, SPI and UART functions as described in Table 2.1. GPIO pins may be configured as inputs or outputs, with a weak pull-up, and with two drive strengths. In addition, PWM, SPI and UART functions may be multiplexed on the pins through the GPIO control register. Please refer to the FE310-G002 Manual for information on GPIO capabilities.
2.8 AON Block Interface Pins

The following pins interface to the Always-ON (AON) block.

- **AON_PMU_OUT_0 (22)**: Programmable SLEEP control OUTPUT
- **AON_PMU_OUT_1 (17)**: Programmable SLEEP control OUTPUT
- **AON_PMU_DWAKEUP_N (18)**: Digital Wake-From-Sleep INPUT, active LOW.
- **AON_ERST_N (24)**: External System Reset INPUT, active LOW.
- **AON_PSD_LFALTCLK (20)**: Optional 32kHz Clock Input.
- **AON_PSD_LFCLKSEL (21)**: 32kHz Clock Source Selector. When driven low, AON PSD LFALTCLK input is used as the 32 kHz low-frequency clock source. When left unconnected or driven high, the internal LFROSC source is used.

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>GPIO</th>
<th>PWM</th>
<th>SPI</th>
<th>UART</th>
<th>I2C</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_0</td>
<td>25</td>
<td>0 I/O</td>
<td>PWM0_0</td>
<td>SPI1_SS0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_1</td>
<td>26</td>
<td>1 I/O</td>
<td>PWM0_1</td>
<td>SPI1_MOSI</td>
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<td></td>
</tr>
<tr>
<td>GPIO_2</td>
<td>27</td>
<td>2 I/O</td>
<td>PWM0_2</td>
<td>SPI1_MISO</td>
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<td></td>
</tr>
<tr>
<td>GPIO_3</td>
<td>28</td>
<td>3 I/O</td>
<td>PWM0_3</td>
<td>SPI1_SCK</td>
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<td></td>
</tr>
<tr>
<td>GPIO_4</td>
<td>29</td>
<td>4 I/O</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_5</td>
<td>31</td>
<td>5 I/O</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>GPIO_6</td>
<td>32</td>
<td>6 I/O</td>
<td>SPI1_SS2</td>
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<td></td>
<td></td>
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<tr>
<td>GPIO_9</td>
<td>33</td>
<td>9 I/O</td>
<td>SPI1_SS2</td>
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<td></td>
<td></td>
</tr>
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<td>GPIO_10</td>
<td>34</td>
<td>10 I/O</td>
<td>PWMI_0</td>
<td>SPI1_SS2</td>
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<td></td>
</tr>
<tr>
<td>GPIO_11</td>
<td>35</td>
<td>11 I/O</td>
<td>PWMI_0</td>
<td>SPI1_SS2</td>
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<td></td>
</tr>
<tr>
<td>GPIO_12</td>
<td>36</td>
<td>12 I/O</td>
<td>PWMI_0</td>
<td>SPI1_SS2</td>
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<td></td>
</tr>
<tr>
<td>GPIO_13</td>
<td>37</td>
<td>13 I/O</td>
<td>PWMI_0</td>
<td>SPI1_SS2</td>
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<td></td>
</tr>
<tr>
<td>GPIO_16</td>
<td>38</td>
<td>16 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_17</td>
<td>39</td>
<td>17 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
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<td>GPIO_18</td>
<td>40</td>
<td>18 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_19</td>
<td>41</td>
<td>19 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
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<td></td>
</tr>
<tr>
<td>GPIO_20</td>
<td>42</td>
<td>20 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_21</td>
<td>43</td>
<td>21 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_22</td>
<td>44</td>
<td>22 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO_23</td>
<td>45</td>
<td>23 I/O</td>
<td>PWMI_1</td>
<td>SPI1_SS2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1: GPIO pin assignments.
Chapter 3

Configuration and Block Diagram

3.1 Block Diagram
Figure 3.1 shows the overall block diagram of FE310-G002. FE310-G002 contains an E31 Core Complex, a selection of flexible I/O peripherals, a dedicated off-chip Quad-SPI flash controller for execute-in-place, 8 KiB of in-circuit programmable OTP memory, 8 KiB of mask ROM, clock generation, and an always-on (AON) block including a programmable power-management unit (PMU).

3.2 E31 Core Complex Configuration
The core is configured to support the RV32IMAC ISA options.
The branch predictor configuration has 40 branch-target buffer (BTB) entries, 128 branch-history (BHT) entries, and a two-entry return-address stack (RAS).
The integer multiplier completes 8 bits per cycle, so takes up to four clock cycles for a single $32 \times 32$ multiply operation.
The integer divider completes one bit per clock cycle, with an early out.
The instruction cache is a 16 KiB two-way set associative with 32-byte lines.
The data SRAM is 16 KiB.
The system mask ROM is 8 KiB in size and contains simple boot code. The system ROM also holds the platform configuration string and debug ROM routines.

3.3 CLINT
The Core Local Interrupt Controller (CLINT) supports the standard timer and software interrupts.

3.4 PLIC
The platform-level interrupt controller (PLIC) receives interrupt signals from the peripheral devices and prioritizes these for service by the core. The PLIC supports 7 programmable priority levels. Please refer to the chapter “FE310-G002 Interrupts” in the SiFive FE310-G002 Manual for more information on the PLIC implementation.
3.5 JTAG Connections
A four-wire 1149.1 JTAG connection is used to connect the external debugger to the internal debug module.

3.6 Debug Module
The debug module is accessed over JTAG, and has support for eight programmable hardware breakpoints.

3.7 Quad-SPI Flash
A dedicated quad-SPI (QSPI) flash interface is provided to hold code and data for the system. The QSPI interface supports burst reads of 32 bytes over TileLink to accelerate instruction cache refills. The QSPI can be programmed to support execute-in-place modes to reduce SPI command overhead on instruction cache refills. The QSPI interface also supports single-word data reads.
over the primary TileLink interface, as well as programming operations using memory-mapped control registers.

3.8 GPIO Complex

The GPIO complex manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. FE310-G002 has two additional QSPI controllers in the GPIO block, one with four chip selects and one with one. FE310-G002 also has two UARTs. FE310-G002 has three PWM controllers, two with 16-bit precision and one with 8-bit precision.

3.9 Always-On (AON) Block

The AON block contains the reset logic for the chip, an on-chip low-frequency oscillator, a watchdog timer, connections for an off-chip low-frequency clock source, the real-time clock, a programmable power-management unit, and 16×32-bit backup registers that retain state while the rest of the chip is powered down.

The AON can be instructed to put the system to sleep. The AON can be programmed to exit sleep mode on a real-time clock interrupt or when the external digital wakeup pin, \texttt{dwakeup\_n}, is pulled low. The \texttt{dwakeup\_n} input supports wired-OR connections of multiple wakeup sources.

3.10 Power Supply

FE310-G002 requires two dedicated power rails providing 1.8 V power to the core logic, and 3.3 V to the I/O pads and to the always on-block.
Chapter 4

FE310-G002 Typical Electrical Specifications

Note: These electrical specifications are TYPICAL ONLY, and are not thoroughly tested in engineering sample parts. Production versions of the devices will be provided with a complete electrical specification. Except where otherwise noted, the typical electrical parameters are specified under the following conditions: Ambient Temperature 27°C, VDD Supply Voltage 1.8V, IVDD Supply Voltage 3.3V, Processor Clock 16MHz crystal. These are preliminary specifications and are subject to change without notice based on characterization.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IVDD</td>
<td>IVDD Supply Current</td>
<td>ACTIVE, 16MHz</td>
<td></td>
<td></td>
<td>8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ACTIVE, 250MHz</td>
<td></td>
<td>16</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IVDD</td>
<td>VDD Supply Current</td>
<td>ACTIVE, 16MHz</td>
<td></td>
<td>8</td>
<td>150</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ACTIVE, 250MHz</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4.1: FE310-G002 Supply Voltage and Current Characteristics
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Voltage LOW Threshold</td>
<td>GPIO, DS=0, 1mA DC Load</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VH</td>
<td>Input Voltage HIGH Threshold</td>
<td>GPIO, DS=1, 1mA DC Load</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Voltage LOW</td>
<td>GPIO, DS=0, 1mA DC Load</td>
<td>20</td>
<td>16</td>
<td>380</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GPIO, DS=0, 20mA DC Load</td>
<td>280</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>VOH</td>
<td>Output Voltage HIGH, with respect to VDDIO</td>
<td>GPIO, DS=0, 1mA DC Load</td>
<td>-18</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GPIO, DS=0, 20mA DC Load</td>
<td>-14</td>
<td>400</td>
<td>-290</td>
<td>mV</td>
</tr>
<tr>
<td>IOL</td>
<td>Output Current LOW</td>
<td>GPIO, DS=0, VGPIO=0.3V</td>
<td>16</td>
<td>21</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IOH</td>
<td>Output Current HIGH</td>
<td>GPIO, DS=0, VGPIO=3.0V</td>
<td>-15</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IPUL</td>
<td>Output Pull-Up Current (PUE=1)</td>
<td>GPIO, VGPIO=0V</td>
<td>-85</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GPIO, VGPIO=2V</td>
<td>-75</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td>ILKH</td>
<td>Input Leakage, HIGH</td>
<td>GPIO, VGPIO=3.3V</td>
<td>200</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>ILKL</td>
<td>Input Leakage, LOW</td>
<td>GPIO, VGPIO=0V</td>
<td>-100</td>
<td></td>
<td></td>
<td>pA</td>
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</table>

**Table 4.2: FE310-G002 Input/Output Characteristics**

<table>
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<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLFRO</td>
<td>Low Frequency Ring Oscillator Center Frequency</td>
<td></td>
<td></td>
<td>40</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>FHFRO</td>
<td>High Frequency Ring Oscillator Center Frequency</td>
<td></td>
<td></td>
<td>72</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>FMAX</td>
<td>Maximum Tested Operating Frequency</td>
<td></td>
<td></td>
<td>320</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

**Table 4.3: FE310-G002 AC Characteristics**
5.1 Boot Code

The FE310-G002 boots by jumping to the beginning of the OTP memory and executing code found there. As shipped, the OTP memory at the boot location is preprogrammed to jump immediately to the end of the OTP memory, which contains the following code to jump to the beginning of the SPI-Flash at 0x2000_0000:

\[
\text{fence 0,0} \\
\text{li \ t0, 0x20000000} \\
\text{jr \ t0}
\]

\text{fence 0,0} is encoded as 0x0000_000F, and the instruction may be modified by burning additional bits to transform it into a JAL instruction ( opcode 0x6F ) to execute arbitrary code rather than jumping directly to the beginning of the SPI-Flash.

Please refer to the OTP Memory section of this datasheet for more information on programming the OTP.
5.2 Trimmed Values

As shipped the OTP memory contains the following information:

<table>
<thead>
<tr>
<th>Item</th>
<th>OTP Address</th>
<th>Factory Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>0</td>
<td>0x7f50_106f</td>
<td>Code to jump to LAST FENCE</td>
</tr>
<tr>
<td>LIFECYCLE</td>
<td>2044</td>
<td>0x1</td>
<td>OTP Lifecycle Counter</td>
</tr>
<tr>
<td>HFROSC TRIM</td>
<td>2043</td>
<td>Varies</td>
<td>HFROSC trim value</td>
</tr>
<tr>
<td>STAMP</td>
<td>2041</td>
<td>Varies</td>
<td>Device ID Stamp, not guaranteed unique.</td>
</tr>
<tr>
<td>LAST FENCE</td>
<td>2045</td>
<td>0x0000_000F</td>
<td>Code to jump to SPI-FLASH.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x2000_02b7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0002_8067</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.1: FE310-G002 OTP Contents as Shipped
6.1 OTP Programming Warnings

**Warning:** Improper use of the One Time Programmable (OTP) memory may result in a nonfunctional device and/or unreliable operation.

- OTP Memory must be programmed following the procedure outlined below *exactly*.
- OTP Memory is designed to be programmed or accessed only while the system clock is running between 1MHz and 37MHz.
- OTP Memory must be programmed only while the power supply voltages remain within specification.

6.2 OTP Programming Procedure

1. LOCK the otp:
   
   (a) Writing 0x1 to `otp_lock`
   
   (b) **Check that 0x1 is read back from** `otp_lock`.
   
   (c) Repeat this step until 0x1 is read successfully.

2. SET the programming voltages by writing the following values:

   ```
   otp_mrr=0x4
   otp_mpp=0x0
   otp_vppen=0x0
   ```

3. WAIT 20us for the programming voltages to stabilize

4. ADDRESS the memory by setting `otp_a`

5. WRITE **one bit at a time**:

   (a) set only the bit you want to write high in `otp_d`
   
   (b) Bring `otp_ck` HIGH for 50us
(c) Bring \texttt{otp.ck} LOW.

Note that this means \textbf{only} one bit of \texttt{otp.d} should be high at any time.

6. VERIFY the written bits setting \texttt{otp.mrr=0x9} for read margin.

7. SOAK any verification failures by repeating steps 2-5 using 400us pulses.

8. REVERIFY the rewritten bits setting \texttt{otp.mrr=0xF}. Steps 7, 8 may be repeated up to 10 times before failing the part.

9. UNLOCK the otp by writing \texttt{0x0} to \texttt{otp.lock}.
Chapter 7

FE310-G002 Package Information

7.1 Package Outline Drawing - 48QFN

The FE310-G002 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) should be connected directly to the ground plane.

Figure 7.1: 48QFN Package Outline Drawing (0.4mm pitch)
7.2 Recommended PCB Footprint - 48QFN

Figure 7.2: 48QFN PCB Footprint Drawing (0.4mm pitch)

NOTE: All Dimensions in mm.