SiFive U54-MC Core Complex Manual

v19.02

SiFive U54-MC Core Complex Manual

Proprietary Notice

Release Information

Version	Date	Changes
v19.02	February 28, 2019	• Changed the date based release numbering system • Top-level module name [U54MC_CoreIPSubsystem] • SiFive Insight [enabled] • WFI-based clock-gating [enabled] • Core local interrupts [16 ⇒ 0] • Global interrupts [128 ⇒ 127]
v1p0	October 10, 2018	• Initial release

Contents

Chapter 1

Introduction

SiFive's U54-MC Core Complex is a high performance, full-Linux-capable, cache-coherent 64-bit RISC-V multiprocessor available as an IP block. The SiFive U54-MC Core Complex is guaranteed to be compatible with all applicable RISC-V standards, and this document should be read together with the official RISC-V user-level, privileged, and external debug architecture specifications.

A summary of features in the U54-MC Core Complex can be found in Table 1.

U54-MC Core Complex Feature Set	
Feature	**Description**
Number of Harts	5 Harts.
S51 Core	1× S51 RISC-V core.
U54 Core	4× U54 RISC-V cores.
PLIC Interrupts	136 Interrupt signals which can be connected to off core complex devices.
PLIC Priority Levels	The PLIC supports 7 priority levels.
Hardware Breakpoints	2 hardware breakpoints.
Physical Memory Protection Unit	PMP with 8 x regions and a minimum granularity of 4 bytes.

Table 1: U54-MC Core Complex Feature Set

1.1 U54-MC Core Complex Overview

An overview of the SiFive U54-MC Core Complex is shown in Figure 1. This RISC-V Core IP includes 5 x 64-bit RISC-V cores, including local and global interrupt support, and physical memory protection. The memory system consists of Data Cache, Data Tightly-Integrated Memory, and Instruction Tightly-Integrated Memory. The U54-MC Core Complex also includes a debug unit, one incoming Port, and three outgoing Ports.

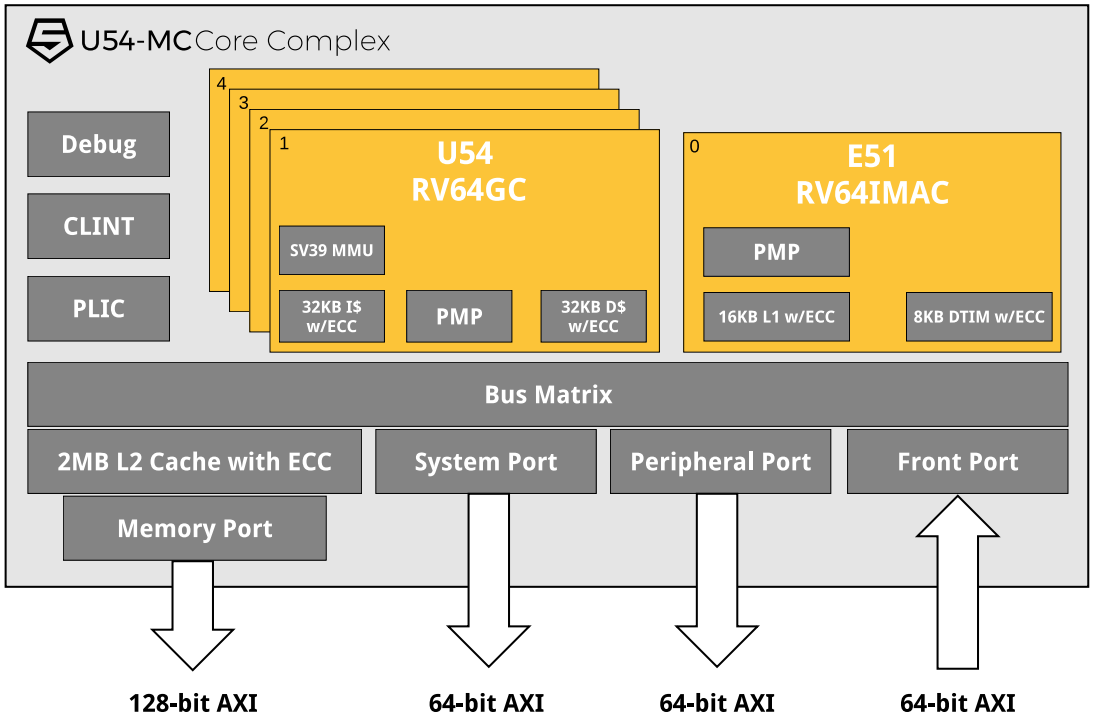

Figure 1: U54-MC Core Complex Block Diagram

The U54-MC Core Complex memory map is detailed in Chapter 5, and the interfaces are described in full in the U54-MC Core Complex User Guide.

1.2 S51 RISC-V Core

The U54-MC Core Complex includes a 64-bit S51 RISC-V core, which has a high-performance single-issue in-order execution pipeline, with a peak sustainable execution rate of one instruction per clock cycle. The S51 core supports Machine and User privilege modes as well as standard Multiply, Atomic, and Compressed RISC-V extensions (RV64IMAC).

The core is described in more detail in Chapter 3.

1.3 U54 RISC-V Cores

The U54-MC Core Complex includes four 64-bit U54 RISC-V cores, which each have a high-performance single-issue in-order execution pipeline, with a peak sustainable execution rate of one instruction per clock cycle. The U54 core supports Machine, Supervisor, and User privilege modes as well as standard Multiply, Single-Precision Floating Point, Double-Precision Floating Point, Atomic, and Compressed RISC-V extensions (RV64IMAFDC).

The cores are described in more detail in Chapter 4.

1.4 Debug Support

The U54-MC Core Complex provides external debugger support over an industry-standard JTAG port, including 2 hardware-programmable breakpoints per hart.

Debug support is described in detail in Chapter 12, and the debug interface is described in the U54-MC Core Complex User Guide.

1.5 Bus-Error Unit

The U54-MC Core Complex has a Bus-Error Unit (BEU) per processor in the core complex which is responsible for recording and reporting error events in the system. The BEU can be configured to generate interrupts on correctable memory errors, uncorrectable memory errors, and/or TileLink bus errors.

More information on the BEU can be found in Chapter 7.

1.6 Interrupts

This Core Complex includes a RISC-V standard platform-level interrupt controller (PLIC), which supports 136 global interrupts with 7 priority levels.

This Core Complex also provides the standard RISC-V machine-mode timer and software interrupts via the Core-Local Interruptor (CLINT).

Interrupts are described in Chapter 6. The CLINT is described in Chapter 8. The PLIC is described in Chapter 9.

Chapter 2

List of Abbreviations and Terms

Term	Definition
BHT	Branch History Table
BTB	Branch Target Buffer
RAS	Return-Address Stack
CLINT	Core-Local Interruptor. Generates per-hart software interrupts and timer interrupts.
CLIC	Core-Local Interrupt Controller. Configures priorities and levels for core local interrupts.
hart	HARdware Thread
DTIM	Data Tightly Integrated Memory
ITIM	Instruction Tightly Integrated Memory
JTAG	Joint Test Action Group
LIM	Loosely Integrated Memory. Used to describe memory space delivered in a SiFive Core Complex but not tightly integrated to a CPU core.
PMP	Physical Memory Protection
PLIC	Platform-Level Interrupt Controller. The global interrupt controller in a RISC-V system.
TileLink	A free and open interconnect standard originally developed at UC Berkeley.
RO	Used to describe a Read Only register field.
RW	Used to describe a Read/Write register field.
WO	Used to describe a Write Only registers field.
WARL	Write-Any Read-Legal field. A register field that can be written with any value, but returns only supported values when read.
WIRI	Writes-Ignored, Reads-Ignore field. A read-only register field reserved for future use. Writes to the field are ignored, and reads should ignore the value returned.
WLRL	Write-Legal, Read-Legal field. A register field that should only be written with legal values and that only returns legal value if last written with a legal value.
WPRI	Writes-Preserve Reads-Ignore field. A register field that might contain unknown information. Reads should ignore the value returned, but writes to the whole register should preserve the original value.

Chapter 3

S51 RISC-V Core

This chapter describes the 64-bit S51 RISC-V processor core used in the U54-MC Core Complex. The S51 processor core comprises an instruction memory system, an instruction fetch unit, an execution pipeline, a data memory system, and support for global, software, and timer interrupts.

The S51 feature set is summarized in Table 2.

Feature	Description
ISA	RV64IMAC.
Instruction Cache	16 KiB 2-way instruction cache.
Instruction Tightly Integrated Memory	The S51 has support for an ITIM with a maximum size of 8 KiB.
Data Tightly Integrated Memory	8 KiB DTIM.
ECC Support	Single error correction, double error detection on the ITIM and DTIM.
Modes	The S51 supports the following modes: Machine Mode, User Mode.

Table 2: S51 Feature Set

3.1 Instruction Memory System

The instruction memory system consists of a dedicated 16 KiB 2-way set-associative instruction cache. The access latency of all blocks in the instruction memory system is one clock cycle. The instruction cache is not kept coherent with the rest of the platform memory system. Writes to instruction memory must be synchronized with the instruction fetch stream by executing a FENCE.I instruction.

The instruction cache has a line size of 64 bytes, and a cache line fill triggers a burst access outside of the U54-MC Core Complex. The core caches instructions from executable addresses, with the exception of the Instruction Tightly Integrated Memory (ITIM), which is further described

in Section 3.1.1. See the U54-MC Core Complex Memory Map in Chapter 5 for a description of executable address regions that are denoted by the attribute X.

Trying to execute an instruction from a non-executable address results in a synchronous trap.

3.1.1 I-Cache Reconfigurability

The instruction cache can be partially reconfigured into ITIM, which occupies a fixed address range in the memory map. ITIM provides high-performance, predictable instruction delivery. Fetching an instruction from ITIM is as fast as an instruction-cache hit, with no possibility of a cache miss. ITIM can hold data as well as instructions, though loads and stores from a core to its ITIM are not as performant as loads and stores to its Data Tightly Integrated Memory (DTIM). Memory requests from one core to any other core's ITIM are not as performant as memory requests from a core to its own ITIM.

The instruction cache can be configured as ITIM for all ways except for 1 in units of cache lines (64 bytes). A single instruction cache way must remain an instruction cache. ITIM is allocated simply by storing to it. A store to the n^{th} byte of the ITIM memory map reallocates the first $n+1$ bytes of instruction cache as ITIM, rounded up to the next cache line.

ITIM is deallocated by storing zero to the first byte after the ITIM region, that is, 8 KiB after the base address of ITIM as indicated in the Memory Map in Chapter 5. The deallocated ITIM space is automatically returned to the instruction cache.

For determinism, software must clear the contents of ITIM after allocating it. It is unpredictable whether ITIM contents are preserved between deallocation and allocation.

3.2 Instruction Fetch Unit

The S51 instruction fetch unit contains branch prediction hardware to improve performance of the processor core. The branch predictor comprises a 28-entry branch target buffer (BTB) which predicts the target of taken branches, a 512-entry branch history table (BHT), which predicts the direction of conditional branches, and a 6-entry return-address stack (RAS) which predicts the target of procedure returns. The branch predictor has a one-cycle latency, so that correctly predicted control-flow instructions result in no penalty. Mispredicted control-flow instructions incur a three-cycle penalty.

The S51 implements the standard Compressed (C) extension to the RISC-V architecture, which allows for 16-bit RISC-V instructions.

3.3 Execution Pipeline

The S51 execution unit is a single-issue, in-order pipeline. The pipeline comprises five stages: instruction fetch, instruction decode and register fetch, execute, data memory access, and register writeback.

The pipeline has a peak execution rate of one instruction per clock cycle, and is fully bypassed so that most instructions have a one-cycle result latency. There are several exceptions:

- LW has a two-cycle result latency, assuming a cache hit.
- LH, LHU, LB, and LBU have a three-cycle result latency, assuming a cache hit.
- CSR reads have a three-cycle result latency.
- MUL, MULH, MULHU, and MULHSU have a 1-cycle result latency.
- DIV, DIVU, REM, and REMU have between a 2-cycle and 64-cycle result latency, depending on the operand values.

The pipeline only interlocks on read-after-write and write-after-write hazards, so instructions may be scheduled to avoid stalls.

The S51 implements the standard Multiply (M) extension to the RISC-V architecture for integer multiplication and division. The S51 has a 64-bit per cycle hardware multiply and a 1-bit per cycle hardware divide. The multiplier can only execute one operation at a time and will block until the previous operation completes.

The hart will not abandon a Divide instruction in flight. This means if an interrupt handler tries to use a register that is the destination register of a divide instruction the pipeline stalls until the divide is complete.

Branch and jump instructions transfer control from the memory access pipeline stage. Correctly-predicted branches and jumps incur no penalty, whereas mispredicted branches and jumps incur a three-cycle penalty.

Most CSR writes result in a pipeline flush with a five-cycle penalty.

3.4 Data Memory System

The S51 data memory system consists of a DTIM interface, which supports up to 8 KiB. The access latency from a core to its own DTIM is two clock cycles for full words and three clock cycles for smaller quantities. Memory requests from one core to any other core's DTIM are not as performant as memory requests from a core to its own DTIM. Misaligned accesses are not supported in hardware and result in a trap to allow software emulation.

Stores are pipelined and commit on cycles where the data memory system is otherwise idle. Loads to addresses currently in the store pipeline result in a five-cycle penalty.

3.5 Atomic Memory Operations

The S51 core supports the RISC-V standard Atomic (A) extension on the DTIM and the Peripheral Port. Atomic memory operations to regions that do not support them generate an access exception precisely at the core.

The load-reserved and store-conditional instructions are only supported on cached regions, hence generate an access exception on DTIM and other uncached memory regions.

See *The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.1* for more information on the instructions added by this extension.

3.6 Supported Modes

The S51 supports RISC-V user mode, providing two levels of privilege: machine (M) and user (U). U-mode provides a mechanism to isolate application processes from each other and from trusted code running in M-mode.

See *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10* for more information on the privilege modes.

3.7 Physical Memory Protection (PMP)

The S51 includes a Physical Memory Protection (PMP) unit compliant with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*. PMP can be used to set memory access privileges (read, write, execute) for specified memory regions. The S51 PMP supports 8 regions with a minimum region size of 4 bytes.

This section describes how PMP concepts in the RISC-V architecture apply to the S51. The definitive resource for information about the RISC-V PMP is *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

3.7.1 Functional Description

The S51 includes a PMP unit, which can be used to restrict access to memory and isolate processes from each other.

The S51 PMP unit has 8 regions and a minimum granularity of 4 bytes. Overlapping regions are permitted. The S51 PMP unit implements the architecturally defined `pmpcfgX` CSR `pmpcfg0` supporting 8 regions. `pmpcfg1`, `pmpcfg2`, and `pmpcfg3` are implemented but hardwired to zero.

The PMP registers may only be programmed in M-mode. Ordinarily, the PMP unit enforces permissions on U-mode accesses. However, locked regions (see Section 3.7.2) additionally enforce their permissions on M-mode.

3.7.2 Region Locking

The PMP allows for region locking whereby, once a region is locked, further writes to the configuration and address registers are ignored. Locked PMP entries may only be unlocked with a system reset. A region may be locked by setting the `L` bit in the pmpicfg register.

In addition to locking the PMP entry, the `L` bit indicates whether the R/W/X permissions are enforced on M-Mode accesses. When the `L` bit is clear, the R/W/X permissions apply only to U-mode.

3.8 Hardware Performance Monitor

The U54-MC Core Complex supports a basic hardware performance monitoring facility compliant with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*. The `mcycle` CSR holds a count of the number of clock cycles the hart has executed since some arbitrary time in the past. The `minstret` CSR holds a count of the number of instructions the hart has retired since some arbitrary time in the past. Both are 64-bit counters.

The hardware performance monitor includes two additional event counters, `mhpmcounter3` and `mhpmcounter4`. The event selector CSRs `mhpmevent3` and `mhpmevent4` are registers that control which event causes the corresponding counter to increment. The `mhpmcounters` are 40-bit counters.

The event selectors are partitioned into two fields, as shown in Table 3: the lower 8 bits select an event class, and the upper bits form a mask of events in that class. The counter increments if the event corresponding to any set mask bit occurs. For example, if `mhpmevent3` is set to `0x4200`, then `mhpmcounter3` will increment when either a load instruction or a conditional branch instruction retires. An event selector of 0 means "count nothing."

Note that in-flight and recently retired instructions may or may not be reflected when reading or writing the performance counters or writing the event selectors.

Machine Hardware Performance Monitor Event Register	
Instruction Commit Events, `mhpeventX`[7:0] = 0	
Bits	**Meaning**
8	Exception taken
9	Integer load instruction retired
10	Integer store instruction retired
11	Atomic memory operation retired
12	System instruction retired
13	Integer arithmetic instruction retired
14	Conditional branch retired
15	JAL instruction retired
16	JALR instruction retired
17	Integer multiplication instruction retired
18	Integer division instruction retired
Microarchitectural Events , `mhpeventX`[7:0] = 1	
Bits	**Meaning**
8	Load-use interlock
9	Long-latency interlock
10	CSR read interlock
11	Instruction cache/ITIM busy
12	Data cache/DTIM busy
13	Branch direction misprediction
14	Branch/jump target misprediction
15	Pipeline flush from CSR write
16	Pipeline flush from other event
17	Integer multiplication interlock
Memory System Events, `mhpeventX`[7:0] = 2	
Bits	**Meaning**
8	Instruction cache miss
9	Memory-mapped I/O access

Table 3: `mhpmevent` Register Description

3.9 ECC

The S51 Instruction Cache and ITIM implement Single-Error Correcting and Double-Error Detecting (SECDED) Error Correcting Code. The granularity at which this protection is applied (the codeword) is 32-bit (with an ECC overhead of 7 bits per codeword).

3.9.1 Single Bit Errors

In the case of a single-bit error in the L1 Instruction Cache, the error is corrected, and the cache line is flushed. When a single-bit error is detected in the ITIM or the DTIM, the error is corrected and written back to the SRAM.

Chapter 4

U54 RISC-V Core

This chapter describes the 64-bit U54 RISC-V processor core used in the U54-MC Core Complex. The U54 processor core comprises an instruction memory system, an instruction fetch unit, an execution pipeline, a floating-point unit, a data memory system, a memory management unit, and support for global, software, and timer interrupts.

The U54 feature set is summarized in Table 4.

Feature	Description
ISA	RV64IMAFDC.
Instruction Cache	32 KiB 8-way instruction cache.
Instruction Tightly Integrated Memory	The U54 has support for an ITIM with a maximum size of 28 KiB.
Data Cache	32 KiB 8-way data cache.
ECC Support	Single error correction, double error detection on the ITIM and Data Cache.
Virtual Memory Support	The U54 has support for Sv39 virtual memory support with a 39-bit virtual address space, 38-bit physical address space, and a 32-entry TLB.
Modes	The U54 supports the following modes: Machine Mode, Supervisor Mode, User Mode.

Table 4: U54 Feature Set

4.1 Instruction Memory System

The instruction memory system consists of a dedicated 32 KiB 8-way set-associative instruction cache. The access latency of all blocks in the instruction memory system is one clock cycle. The instruction cache is not kept coherent with the rest of the platform memory system. Writes to instruction memory must be synchronized with the instruction fetch stream by executing a FENCE.I instruction.

The instruction cache has a line size of 64 bytes, and a cache line fill triggers a burst access outside of the U54-MC Core Complex. The core caches instructions from executable addresses, with the exception of the Instruction Tightly Integrated Memory (ITIM), which is further described in Section 3.1.1. See the U54-MC Core Complex Memory Map in Chapter 5 for a description of executable address regions that are denoted by the attribute X.

Trying to execute an instruction from a non-executable address results in a synchronous trap.

4.1.1 I-Cache Reconfigurability

The instruction cache can be partially reconfigured into ITIM, which occupies a fixed address range in the memory map. ITIM provides high-performance, predictable instruction delivery. Fetching an instruction from ITIM is as fast as an instruction-cache hit, with no possibility of a cache miss. ITIM can hold data as well as instructions, though loads and stores from a core to its ITIM are not as performant as hits in the D-Cache. Memory requests from one core to any other core's ITIM are not as performant as memory requests from a core to its own ITIM.

The instruction cache can be configured as ITIM for all ways except for 1 in units of cache lines (64 bytes). A single instruction cache way must remain an instruction cache. ITIM is allocated simply by storing to it. A store to the n^{th} byte of the ITIM memory map reallocates the first $n+1$ bytes of instruction cache as ITIM, rounded up to the next cache line.

ITIM is deallocated by storing zero to the first byte after the ITIM region, that is, 28 KiB after the base address of ITIM as indicated in the Memory Map in Chapter 5. The deallocated ITIM space is automatically returned to the instruction cache.

For determinism, software must clear the contents of ITIM after allocating it. It is unpredictable whether ITIM contents are preserved between deallocation and allocation.

4.2 Instruction Fetch Unit

The U54 instruction fetch unit contains branch prediction hardware to improve performance of the processor core. The branch predictor comprises a 28-entry branch target buffer (BTB) which predicts the target of taken branches, a 512-entry branch history table (BHT), which predicts the direction of conditional branches, and a 6-entry return-address stack (RAS) which predicts the target of procedure returns. The branch predictor has a one-cycle latency, so that correctly predicted control-flow instructions result in no penalty. Mispredicted control-flow instructions incur a three-cycle penalty.

The U54 implements the standard Compressed (C) extension to the RISC-V architecture, which allows for 16-bit RISC-V instructions.

4.3 Execution Pipeline

The U54 execution unit is a single-issue, in-order pipeline. The pipeline comprises five stages: instruction fetch, instruction decode and register fetch, execute, data memory access, and register writeback.

The pipeline has a peak execution rate of one instruction per clock cycle, and is fully bypassed so that most instructions have a one-cycle result latency. There are several exceptions:

- LW has a two-cycle result latency, assuming a cache hit.
- LH, LHU, LB, and LBU have a three-cycle result latency, assuming a cache hit.
- CSR reads have a three-cycle result latency.
- MUL, MULH, MULHU, and MULHSU have a 1-cycle result latency.
- DIV, DIVU, REM, and REMU have between a 2-cycle and 64-cycle result latency, depending on the operand values.

The pipeline only interlocks on read-after-write and write-after-write hazards, so instructions may be scheduled to avoid stalls.

The U54 implements the standard Multiply (M) extension to the RISC-V architecture for integer multiplication and division. The U54 has a 64-bit per cycle hardware multiply and a 1-bit per cycle hardware divide. The multiplier is fully pipelined and can begin a new operation on each cycle, with a maximum throughput of one operation per cycle.

The hart will not abandon a Divide instruction in flight. This means if an interrupt handler tries to use a register that is the destination register of a divide instruction the pipeline stalls until the divide is complete.

Branch and jump instructions transfer control from the memory access pipeline stage. Correctly-predicted branches and jumps incur no penalty, whereas mispredicted branches and jumps incur a three-cycle penalty.

Most CSR writes result in a pipeline flush with a five-cycle penalty.

4.4 Data Memory System

The U54 data memory system has a 8-way set-associative 32 KiB write-back data cache that supports 64-byte cache lines. The access latency is two clock cycles for words and double-words, and three clock cycles for smaller quantities. Misaligned accesses are not supported in hardware and result in a trap to support software emulation. The data caches are kept coherent with a directory-based cache coherence manager, which resides in the outer L2 cache.

Stores are pipelined and commit on cycles where the data memory system is otherwise idle. Loads to addresses currently in the store pipeline result in a five-cycle penalty.

4.5 Atomic Memory Operations

The U54 core supports the RISC-V standard Atomic (A) extension on the DTIM and the Peripheral Port. Atomic memory operations to regions that do not support them generate an access exception precisely at the core.

The load-reserved and store-conditional instructions are only supported on cached regions, hence generate an access exception on DTIM and other uncached memory regions.

See *The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.1* for more information on the instructions added by this extension.

4.6 Floating-Point Unit (FPU)

The U54 FPU provides full hardware support for the IEEE 754-2008 floating-point standard for 32-bit single-precision and 64-bit double-precision arithmetic. The FPU includes a fully pipelined fused-multiply-add unit and an iterative divide and square-root unit, magnitude comparators, and float-to-integer conversion units, all with full hardware support for subnormals and all IEEE default values.

4.7 Virtual Memory Support

The U54 has support for virtual memory through the use of a Memory Management Unit (MMU). The MMU supports the Bare and Sv39 modes as described in *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

The U54 MMU has a 39 virtual address space mapped to a 38 physical address space. A hardware page-table walker refills the address translation caches. Both first-level instruction and data address translation caches are fully associative and have 32 entries. There is also a unified second-level translation cache with 128 entries. The MMU supports 2 MiB megapages and 1 GiB gigapages to reduce translation overheads for large contiguous regions of virtual and physical address space.

Note that the U54 does not automatically set the **Accessed** (A) and **Dirty** (D) bits in a Sv39 Page Table Entry (PTE). Instead, the U54 MMU will raise a page fault exception for a read to a page with PTE.A=0 or a write to a page with PTE.D=0.

4.8 Supported Modes

The U54 supports RISC-V supervisor and user modes, providing three levels of privilege: machine (M), supervisor (S) and user (U). U-mode provides a mechanism to isolate application processes from each other and from trusted code running in M-mode. S-mode adds a number of additional CSRs and capabilities.

See *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10* for more information on the privilege modes.

4.9 Physical Memory Protection (PMP)

The U54 includes a Physical Memory Protection (PMP) unit compliant with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*. PMP can be used to set memory access privileges (read, write, execute) for specified memory regions. The U54 PMP supports 8 regions with a minimum region size of 4 bytes.

This section describes how PMP concepts in the RISC-V architecture apply to the U54. The definitive resource for information about the RISC-V PMP is *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

4.9.1 Functional Description

The U54 includes a PMP unit, which can be used to restrict access to memory and isolate processes from each other.

The U54 PMP unit has 8 regions and a minimum granularity of 4 bytes. Overlapping regions are permitted. The U54 PMP unit implements the architecturally defined `pmpcfgX` CSR `pmpcfg0` supporting 8 regions. `pmpcfg1`, `pmpcfg2`, and `pmpcfg3` are implemented but hardwired to zero.

The PMP registers may only be programmed in M-mode. Ordinarily, the PMP unit enforces permissions on S-mode and U-mode accesses. However, locked regions (see Section 3.7.2) additionally enforce their permissions on M-mode.

4.9.2 Region Locking

The PMP allows for region locking whereby, once a region is locked, further writes to the configuration and address registers are ignored. Locked PMP entries may only be unlocked with a system reset. A region may be locked by setting the `L` bit in the pmpicfg register.

In addition to locking the PMP entry, the `L` bit indicates whether the R/W/X permissions are enforced on M-Mode accesses. When the `L` bit is clear, the R/W/X permissions apply to S-mode and U-mode.

4.10 Hardware Performance Monitor

The U54-MC Core Complex supports a basic hardware performance monitoring facility compliant with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*. The `mcycle` CSR holds a count of the number of clock cycles the hart has executed since some arbitrary time in the past. The `minstret` CSR holds a count of the number of instructions the hart has retired since some arbitrary time in the past. Both are 64-bit counters.

The hardware performance monitor includes two additional event counters, `mhpmcounter3` and `mhpmcounter4`. The event selector CSRs `mhpmevent3` and `mhpmevent4` are registers that control which event causes the corresponding counter to increment. The `mhpmcounters` are 40-bit counters.

The event selectors are partitioned into two fields, as shown in Table 5: the lower 8 bits select an event class, and the upper bits form a mask of events in that class. The counter increments if the event corresponding to any set mask bit occurs. For example, if `mhpmevent3` is set to `0x4200`, then `mhpmcounter3` will increment when either a load instruction or a conditional branch instruction retires. An event selector of 0 means "count nothing."

Note that in-flight and recently retired instructions may or may not be reflected when reading or writing the performance counters or writing the event selectors.

Machine Hardware Performance Monitor Event Register	
Instruction Commit Events, `mhpeventX`[7:0] = 0	
Bits	**Meaning**
8	Exception taken
9	Integer load instruction retired
10	Integer store instruction retired
11	Atomic memory operation retired
12	System instruction retired
13	Integer arithmetic instruction retired
14	Conditional branch retired
15	JAL instruction retired
16	JALR instruction retired
17	Integer multiplication instruction retired
18	Integer division instruction retired
19	Floating-point load instruction retired
20	Floating-point store instruction retired
21	Floating-point addition retired
22	Floating-point multiplication retired
23	Floating-point fused multiply-add retired
24	Floating-point division or square-root retired
25	Other floating-point instruction retired
Microarchitectural Events , `mhpeventX`[7:0] = 1	
Bits	**Meaning**
8	Load-use interlock
9	Long-latency interlock
10	CSR read interlock
11	Instruction cache/ITIM busy
12	Data cache/DTIM busy
13	Branch direction misprediction
14	Branch/jump target misprediction
15	Pipeline flush from CSR write
16	Pipeline flush from other event
17	Integer multiplication interlock
18	Floating-point interlock
Memory System Events, `mhpeventX`[7:0] = 2	
Bits	**Meaning**
8	Instruction cache miss
9	Data cache miss or memory-mapped I/O access
10	Data cache writeback
11	Instruction TLB miss
12	Data TLB miss

Table 5: `mhpmevent` Register Description

4.11 ECC

The U54 Instruction Cache, ITIM, and Data Cache implement Single-Error Correcting and Double-Error Detecting (SECDED) Error Correcting Code. The granularity at which this protection is applied (the codeword) is 32-bit (with an ECC overhead of 7 bits per codeword).

4.11.1 Single Bit Errors

In the case of a single-bit error in the L1 Instruction Cache, the error is corrected, and the cache line is flushed. When a single-bit error is detected in the ITIM, the error is corrected and written back to the SRAM.

When the L1 Data Cache encounters a single-bit error, the Data Cache corrects the error, invalidates the cache line, and writes the line back to the next level of memory hierarchy.

Chapter 5

Memory Map

The memory map of the U54-MC Core Complex is shown in Table 6.

Base	Top	Attr.	Description	Notes
0x0000_0000	0x0000_0FFF	RWX A	Debug	Debug Address Space
0x0000_1000	0x0000_2FFF		Reserved	On Core Complex Address Space
0x0000_3000	0x0000_3FFF	RWX A	Error Device	
0x0000_4000	0x00FF_FFFF		Reserved	
0x0100_0000	0x0100_1FFF	RWX A	Hart 0 Data Tightly-Integrated Memory (DTIM) (8 KiB)	
0x0100_2000	0x016F_FFFF		Reserved	
0x0170_0000	0x0170_0FFF	RW A	Bus-Error Unit 0	
0x0170_1000	0x0170_1FFF	RW A	Bus-Error Unit 1	
0x0170_2000	0x0170_2FFF	RW A	Bus-Error Unit 2	
0x0170_3000	0x0170_3FFF	RW A	Bus-Error Unit 3	
0x0170_4000	0x0170_4FFF	RW A	Bus-Error Unit 4	
0x0170_5000	0x017F_FFFF		Reserved	
0x0180_0000	0x0180_3FFF	RWX A	Hart 0 ITIM (16 KiB)	
0x0180_4000	0x0180_7FFF		Reserved	
0x0180_8000	0x0180_FFFF	RWX A	Hart 1 ITIM (32 KiB)	
0x0181_0000	0x0181_7FFF	RWX A	Hart 2 ITIM (32 KiB)	
0x0181_8000	0x0181_FFFF	RWX A	Hart 3 ITIM (32 KiB)	
0x0182_0000	0x0182_7FFF	RWX A	Hart 4 ITIM (32 KiB)	
0x0182_8000	0x01FF_FFFF		Reserved	
0x0200_0000	0x0200_FFFF	RW A	CLINT	
0x0201_0000	0x0201_0FFF	RW A	Cache Controller	
0x0201_1000	0x07FF_FFFF		Reserved	
0x0800_0000	0x081F_FFFF	RWX A	L2 LIM (2 MiB)	
0x0820_0000	0x09FF_FFFF		Reserved	
0x0A00_0000	0x0BFF_FFFF	RWXCA	L2 Zero device	
0x0C00_0000	0x0FFF_FFFF	RW A	PLIC	
0x1000_0000	0x1F00_0FFF		Reserved	
0x2000_0000	0x3FFF_FFFF	RWX A	Peripheral Port (512 MiB)	Off Core Complex Address Space
0x4000_0000	0x5FFF_FFFF	RWX	System Port (512 MiB)	
0x6000_0000	0x7FFF_FFFF		Reserved	
0x8000_0000	0x9FFF_FFFF	RWXCA	Memory Port (512 MiB)	
0xA000_0000	0xFFFF_FFFF		Reserved	
0x1_0000_0000	0xF_FFFF_FFFF	RWX A	Peripheral Port (60 GiB)	
0x10_0000_0000	0x3F_FFFF_FFFF	RWX	System Port (192 GiB)	

Table 6: U54-MC Core Complex Memory Map. Memory Attributes: **R** - Read, **W** - Write, **X** - Execute, **C** - Cacheable, **A** - Atomics

Chapter 6

Interrupts

This chapter describes how interrupt concepts in the RISC-V architecture apply to the U54-MC Core Complex.

The definitive resource for information about the RISC-V interrupt architecture is *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

6.1 Interrupt Concepts

The U54-MC Core Complex supports Machine Mode and Supervisor Mode interrupts. It also has support for the following types of RISC-V interrupts: local and global.

Local interrupts are signaled directly to an individual hart with a dedicated interrupt value. This allows for reduced interrupt latency as no arbitration is required to determine which hart will service a given request and no additional memory accesses are required to determine the cause of the interrupt.

Software and timer interrupts are local interrupts generated by the Core-Local Interruptor (CLINT). The U54-MC Core Complex contains no other local interrupt sources.

Global interrupts, by contrast, are routed through a Platform-Level Interrupt Controller (PLIC), which can direct interrupts to any hart in the system via the external interrupt. Decoupling global interrupts from the hart(s) allows the design of the PLIC to be tailored to the platform, permitting a broad range of attributes like the number of interrupts and the prioritization and routing schemes.

By default, all interrupts are handled in machine mode. For harts that support supervisor mode, it is possible to selectively delegate interrupts to supervisor mode.

This chapter describes the U54-MC Core Complex interrupt architecture.

Chapter 8 describes the Core-Local Interruptor.

Chapter 9 describes the global interrupt architecture and the PLIC design.

The U54-MC Core Complex interrupt architecture is depicted in Figure 2.

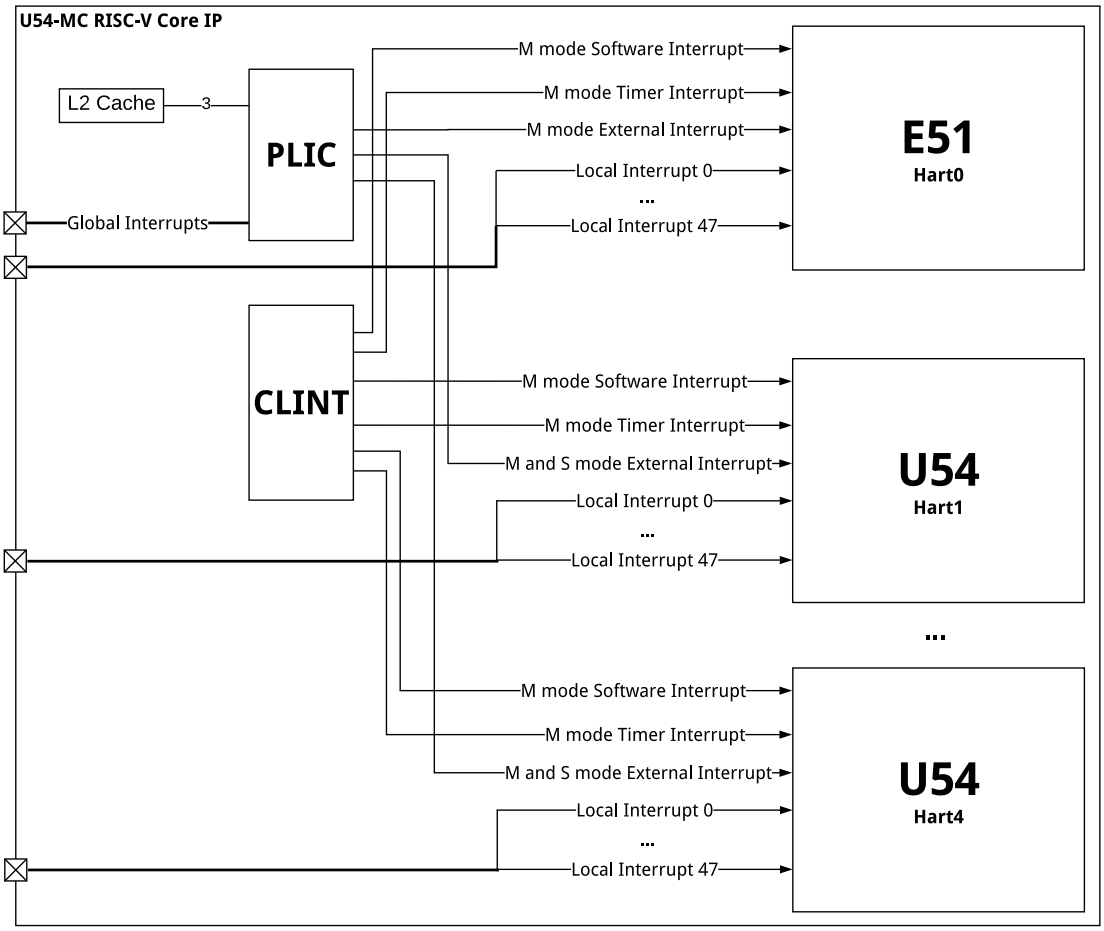

Figure 2: U54-MC Core Complex Interrupt Architecture Block Diagram.

6.2 Interrupt Operation

Within a privilege mode *m*, if the associated global interrupt-enable {ie} is clear, then no interrupts will be taken in that privilege mode, but a pending-enabled interrupt in a higher privilege mode will preempt current execution. If {ie} is set, then pending-enabled interrupts at a higher interrupt level in the same privilege mode will preempt current execution and run the interrupt handler for the higher interrupt level.

When an interrupt or synchronous exception is taken, the privilege mode is modified to reflect the new privilege mode. The global interrupt-enable bit of the handler's privilege mode is cleared.

6.2.1 Interrupt Entry and Exit

When an interrupt occurs:

- The value of `mstatus.MIE` is copied into `mcause.MPIE`, and then `mstatus.MIE` is cleared, effectively disabling interrupts.
- The privilege mode prior to the interrupt is encoded in `mstatus.MPP`.
- The current `pc` is copied into the `mepc` register, and then `pc` is set to the value specified by `mtvec` as defined by the `mtvec.MODE` described in Table 9.

At this point, control is handed over to software in the interrupt handler with interrupts disabled. Interrupts can be re-enabled by explicitly setting `mstatus.MIE` or by executing an `MRET` instruction to exit the handler. When an MRET instruction is executed, the following occurs:

- The privilege mode is set to the value encoded in `mstatus.MPP`.
- The global interrupt enable, `mstatus.MIE`, is set to the value of `mcause.MPIE`.
- The `pc` is set to the value of `mepc`.

At this point control is handed over to software.

The Control and Status Registers involved in handling RISC-V interrupts are described in Section 6.3.

6.3 Interrupt Control Status Registers

The U54-MC Core Complex specific implementation of interrupt CSRs is described below. For a complete description of RISC-V interrupt behavior and how to access CSRs, please consult *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

6.3.1 Machine Status Register (`mstatus`)

The `mstatus` register keeps track of and controls the hart's current operating state, including whether or not interrupts are enabled. A summary of the `mstatus` fields related to interrupts in the U54-MC Core Complex is provided in Table 7. Note that this is not a complete description of `mstatus` as it contains fields unrelated to interrupts. For the full description of `mstatus`, please consult the *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

Machine Status Register			
CSR	`mstatus`		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WPRI	
1	SIE	RW	Supervisor Interrupt Enable
2	Reserved	WPRI	
3	MIE	RW	Machine Interrupt Enable
4	Reserved	WPRI	
5	SPIE	RW	Supervisor Previous Interrupt Enable
6	Reserved	WPRI	
7	MPIE	RW	Machine Previous Interrupt Enable
8	SPP	RW	Supervisor Previous Privilege Mode
[10:9]	Reserved	WPRI	
[12:11]	MPP	RW	Machine Previous Privilege Mode

Table 7: U54-MC Core Complex `mstatus` Register (partial)

Interrupts are enabled by setting the MIE bit in `mstatus` and by enabling the desired individual interrupt in the `mie` register, described in Section 6.3.3.

6.3.2 Machine Trap Vector (`mtvec`)

The `mtvec` register has two main functions: defining the base address of the trap vector, and setting the mode by which the U54-MC Core Complex will process interrupts. The interrupt processing mode is defined in the lower two bits of the `mtvec` register as described in Table 9.

Machine Trap Vector Register			
CSR	`mtvec`		
Bits	**Field Name**	**Attr.**	**Description**
[1:0]	MODE	WARL	`MODE` Sets the interrupt processing mode. The encoding for the U54-MC Core Complex supported modes is described in Table 9.
[63:2]	BASE[63:2]	WARL	Interrupt Vector Base Address. Requires 64-byte alignment.

Table 8: `mtvec` Register

MODE Field Encoding `mtvec.MODE`		
Value	**Name**	**Description**
0x0	Direct	All exceptions set `pc` to `BASE`
0x1	Vectored	Asynchronous interrupts set `pc` to `BASE` + 4 × `mcause.EXCCODE`.
≥ 2	Reserved	

Table 9: Encoding of `mtvec.MODE`

See Table 8 for a description of the mtvec register. See Table 9 for a description of the mtvec.MODE field. See Table 13 for the U54-MC Core Complex interrupt exception code values.

Mode Direct

When operating in direct mode all synchronous exceptions and asynchronous interrupts trap to the mtvec.BASE address. Inside the trap handler, software must read the mcause register to determine what triggered the trap.

Mode Vectored

While operating in vectored mode, interrupts set the pc to mtvec.BASE + 4 × exception code. For example, if a machine timer interrupt is taken, the pc is set to mtvec.BASE + 0x1C. Typically, the trap vector table is populated with jump instructions to transfer control to interrupt-specific trap handlers.

In vectored interrupt mode, BASE must be 64-byte aligned.

All machine external interrupts (global interrupts) are mapped to exception code of 11. Thus, when interrupt vectoring is enabled, the pc is set to address mtvec.BASE + 0x2C for any global interrupt.

6.3.3 Machine Interrupt Enable (mie)

Individual interrupts are enabled by setting the appropriate bit in the mie register. The mie register is described in Table 10.

Machine Interrupt Enable Register			
CSR	mie		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WPRI	
1	SSIE	RW	Supervisor Software Interrupt Enable
2	Reserved	WPRI	
3	MSIE	RW	Machine Software Interrupt Enable
4	Reserved	WPRI	
5	STIE	RW	Supervisor Timer Interrupt Enable
6	Reserved	WPRI	
7	MTIE	RW	Machine Timer Interrupt Enable
8	Reserved	WPRI	
9	SEIE	RW	Supervisor External Interrupt Enable
10	Reserved	WPRI	
11	MEIE	RW	Machine External Interrupt Enable
[63:12]	Reserved	WPRI	

Table 10: mie Register

6.3.4 Machine Interrupt Pending (`mip`)

The machine interrupt pending (`mip`) register indicates which interrupts are currently pending. The `mip` register is described in Table 11.

Machine Interrupt Pending Register			
CSR	`mip`		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WIRI	
1	SSIP	RW	Supervisor Software Interrupt Pending
2	Reserved	WIRI	
3	MSIP	RO	Machine Software Interrupt Pending
4	Reserved	WIRI	
5	STIP	RW	Supervisor Timer Interrupt Pending
6	Reserved	WIRI	
7	MTIP	RO	Machine Timer Interrupt Pending
8	Reserved	WIRI	
9	SEIP	RW	Supervisor External Interrupt Pending
10	Reserved	WIRI	
11	MEIP	RO	Machine External Interrupt Pending
[63:12]	Reserved	WIRI	

Table 11: `mip` Register

6.3.5 Machine Cause (`mcause`)

When a trap is taken in machine mode, `mcause` is written with a code indicating the event that caused the trap. When the event that caused the trap is an interrupt, the most-significant bit of `mcause` is set to 1, and the least-significant bits indicate the interrupt number, using the same encoding as the bit positions in `mip`. For example, a Machine Timer Interrupt causes `mcause` to be set to `0x8000_0000_0000_0007`. `mcause` is also used to indicate the cause of synchronous exceptions, in which case the most-significant bit of `mcause` is set to 0.

See Table 12 for more details about the `mcause` register. Refer to Table 13 for a list of synchronous exception codes.

Machine Cause Register			
CSR	`mcause`		
Bits	**Field Name**	**Attr.**	**Description**
[9:0]	Exception Code	WLRL	A code identifying the last exception.
[62:10]	Reserved	WLRL	
63	Interrupt	WARL	1 if the trap was caused by an interrupt; 0 otherwise.

Table 12: `mcause` Register

Interrupt Exception Codes		
Interrupt	**Exception Code**	**Description**
1	0	Reserved
1	1	Supervisor software interrupt
1	2	Reserved
1	3	Machine software interrupt
1	4	Reserved
1	5	Supervisor timer interrupt
1	6	Reserved
1	7	Machine timer interrupt
1	8	Reserved
1	9	Supervisor external interrupt
1	8	Reserved
1	11	Machine external interrupt
1	≥ 12	Reserved
0	0	Instruction address misaligned
0	1	Instruction access fault
0	2	Illegal instruction
0	3	Breakpoint
0	4	Load address misaligned
0	5	Load access fault
0	6	Store/AMO address misaligned
0	7	Store/AMO access fault
0	8	Environment call from U-mode
0	9	Environment call from S-mode
0	10	Reserved
0	11	Environment call from M-mode
0	12	Instruction page fault
0	13	Load page fault
0	14	Reserved
0	15	Store/AMO page fault
0	≥ 16	Reserved

Table 13: `mcause` Exception Codes

6.4 Supervisor Mode Interrupts

The U54-MC Core Complex supports the ability to selectively direct interrupts and exceptions to supervisor mode, resulting in improved performance by eliminating the need for additional mode changes.

This capability is enabled by the interrupt and exception delegation CSRs; `mideleg` and `medeleg`, respectively. Supervisor interrupts and exceptions can be managed via supervisor versions of the interrupt CSRs, specifically: `stvec`, `sip`, `sie`, and `scause`.

Machine mode software can also directly write to the `sip` register, which effectively sends an interrupt to supervisor mode. This is especially useful for timer and software interrupts as it may be desired to handle these interrupts in both machine mode and supervisor mode.

The delegation and supervisor CSRs are described in the sections below. The definitive resource for information about RISC-V supervisor interrupts is *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

6.4.1 Delegation Registers (`m*deleg`)

By default, all traps are handled in machine mode. Machine mode software can selectively delegate interrupts and exceptions to supervisor mode by setting the corresponding bits in `mideleg` and `medeleg` CSRs. The exact mapping is provided in Table 14 and Table 15 and matches the `mcause` interrupt and exception codes defined in Table 13.

Note that local interrupts can not be delegated to supervisor mode.

Machine Interrupt Delegation Register			
CSR	`mideleg`		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WARL	
1	MSIP	RW	Delegate Supervisor Software Interrupt
[4:2]	Reserved	WARL	
5	MTIP	RW	Delegate Supervisor Timer Interrupt
[8:6]	Reserved	WARL	
9	MEIP	RW	Delegate Supervisor External Interrupt
[63:10]	Reserved	WARL	

Table 14: `mideleg` Register

Machine Exception Delegation Register			
CSR	`medeleg`		
Bits	**Field Name**	**Attr.**	**Description**
0		RW	Delegate Instruction Access Misaligned Exception
1		RW	Delegate Instruction Access Fault Exception
2		RW	Delegate Illegal Instruction Exception
3		RW	Delegate Breakpoint Exception
4		RW	Delegate Load Access Misaligned Exception
5		RW	Delegate Load Access Fault Exception
6		RW	Delegate Store/AMO Address Misaligned Exception
7		RW	Delegate Store/AMO Access Fault Exception
8		RW	Delegate Environment Call from U-Mode
9		RW	Delegate Environment Call from S-Mode
[11:0]	Reserved	WARL	
12		RW	Delegate Instruction Page Fault
13		RW	Delegate Load Page Fault
14	Reserved	WARL	
15		RW	Delegate Store/AMO Page Fault Exception
[63:16]	Reserved	WARL	

Table 15: `medeleg` Register

6.4.2 Supervisor Status Register (`sstatus`)

Similar to machine mode, supervisor mode has a register dedicated to keeping track of the hart's current state called `sstatus`. `sstatus` is effectively a restricted view of `mstatus`, described in Section 6.3.1, in that changes made to `sstatus` are reflected in `mstatus` and vice-versa, with the exception of the machine mode fields, which are not visible in `sstatus`.

A summary of the `sstatus` fields related to interrupts in the U54-MC Core Complex is provided in Table 16. Note that this is not a complete description of `sstatus` as it also contains fields unrelated to interrupts. For the full description of `sstatus`, consult the *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

Supervisor Status Register			
CSR	sstatus		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WPRI	
1	SIE	RW	Supervisor Interrupt Enable
[4:2]	Reserved	WPRI	
5	SPIE	RW	Supervisor Previous Interrupt Enable
[7:6]	Reserved	WPRI	
8	SPP	RW	Supervisor Previous Privilege Mode
[12:9]	Reserved	WPRI	

Table 16: U54-MC Core Complex `sstatus` Register (partial)

Interrupts are enabled by setting the `SIE` bit in `sstatus` and by enabling the desired individual interrupt in the `sie` register, described in Section 6.4.3.

6.4.3 Supervisor Interrupt Enable Register (`sie`)

Supervisor interrupts are enabled by setting the appropriate bit in the `sie` register. The U54-MC Core Complex `sie` register is described in Table 17.

Supervisor Interrupt Enable Register			
CSR	sie		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WPRI	
1	SSIE	RW	Supervisor Software Interrupt Enable
[4:2]	Reserved	WPRI	
5	STIE	RW	Supervisor Timer Interrupt Enable
[8:6]	Reserved	WPRI	
9	SEIE	RW	Supervisor External Interrupt Enable
[63:10]	Reserved	WPRI	

Table 17: `sie` Register

6.4.4 Supervisor Interrupt Pending (`sip`)

The supervisor interrupt pending (`sip`) register indicates which interrupts are currently pending. The U54-MC Core Complex `sip` register is described in Table 18.

Supervisor Interrupt Pending Register			
CSR	`sip`		
Bits	**Field Name**	**Attr.**	**Description**
0	Reserved	WIRI	
1	SSIP	RW	Supervisor Software Interrupt Pending
[4:2]	Reserved	WIRI	
5	STIP	RW	Supervisor Timer Interrupt Pending
[8:6]	Reserved	WIRI	
9	SEIP	RW	Supervisor External Interrupt Pending
[63:10]	Reserved	WIRI	

Table 18: `sip` Register

6.4.5 Supervisor Cause Register (`scause`)

When a trap is taken in supervisor mode, `scause` is written with a code indicating the event that caused the trap. When the event that caused the trap is an interrupt, the most-significant bit of `scause` is set to 1, and the least-significant bits indicate the interrupt number, using the same encoding as the bit positions in `sip`. For example, a Supervisor Timer Interrupt causes `scause` to be set to `0x8000_0000_0000_0005`.

`scause` is also used to indicate the cause of synchronous exceptions, in which case the most-significant bit of `scause` is set to 0. Refer to Table 20 for a list of synchronous exception codes.

Supervisor Cause Register			
CSR	`scause`		
Bits	**Field Name**	**Attr.**	**Description**
[62:0]	Exception Code	WLRL	A code identifying the last exception.
63	Interrupt	WARL	1 if the trap was caused by an interrupt; 0 otherwise.

Table 19: `scause` Register

Supervisor Interrupt Exception Codes		
Interrupt	**Exception Code**	**Description**
1	0	Reserved
1	1	Supervisor software interrupt
1	2 – 4	Reserved
1	5	Supervisor timer interrupt
1	6 – 8	Reserved
1	9	Supervisor external interrupt
1	≥ 10	Reserved
0	0	Instruction address misaligned
0	1	Instruction access fault
0	2	Illegal instruction
0	3	Breakpoint
0	4	Reserved
0	5	Load access fault
0	6	Store/AMO address misaligned
0	7	Store/AMO access fault
0	8	Environment call from U-mode
0	9 – 11	Reserved
0	12	Instruction page fault
0	13	Load page fault
0	14	Reserved
0	15	Store/AMO Page Fault
0	≥ 16	Reserved

Table 20: `scause` Exception Codes

6.4.6 Supervisor Trap Vector (`stvec`)

By default, all interrupts trap to a single address defined in the `stvec` register. It is up to the interrupt handler to read `scause` and react accordingly. RISC-V and the U54-MC Core Complex also support the ability to optionally enable interrupt vectors. When vectoring is enabled, each interrupt defined in `sie` will trap to its own specific interrupt handler.

Vectored interrupts are enabled when the MODE field of the `stvec` register is set to 1.

Supervisor Trap Vector Register			
CSR	stvec		
Bits	**Field Name**	**Attr.**	**Description**
[1:0]	MODE	WARL	MODE determines whether or not interrupt vectoring is enabled. The encoding for the MODE field is described in Table 22.
[63:2]	BASE[63:2]	WARL	Interrupt Vector Base Address. Must be aligned on a 128-byte boundary when MODE=1. Note, BASE[1:0] is not present in this register and is implicitly 0.

Table 21: stvec Register

MODE Field Encoding stvec.MODE		
Value	**Name**	**Description**
0	Direct	All exceptions set pc to BASE
1	Vectored	Asynchronous interrupts set pc to BASE + 4 × cause.
≥ 2	Reserved	

Table 22: Encoding of stvec.MODE

If vectored interrupts are disabled (stvec.MODE=0), all interrupts trap to the stvec.BASE address. If vectored interrupts are enabled (stvec.MODE=1), interrupts set the pc to stvec.BASE + 4 × exception code. For example, if a supervisor timer interrupt is taken, the pc is set to stvec.BASE + 0x14. Typically, the trap vector table is populated with jump instructions to transfer control to interrupt-specific trap handlers.

In vectored interrupt mode, BASE must be 128-byte aligned.

All supervisor external interrupts (global interrupts) are mapped to exception code of 9. Thus, when interrupt vectoring is enabled, the pc is set to address stvec.BASE + 0x24 for any global interrupt.

See Table 21 for a description of the stvec register. See Table 22 for a description of the stvec.MODE field. See Table 20 for the U54-MC Core Complex supervisor mode interrupt exception code values.

6.4.7 Delegated Interrupt Handling

Upon taking a delegated trap, the following occurs:

- The value of sstatus.SIE is copied into sstatus.SPIE, then sstatus.SIE is cleared, effectively disabling interrupts.

- The current pc is copied into the sepc register, and then pc is set to the value of stvec. In the case where vectored interrupts are enabled, pc is set to stvec.BASE + 4 × exception code.
- The privilege mode prior to the interrupt is encoded in sstatus.SPP.

At this point, control is handed over to software in the interrupt handler with interrupts disabled. Interrupts can be re-enabled by explicitly setting sstatus.SIE or by executing an SRET instruction to exit the handler. When an SRET instruction is executed, the following occurs:

- The privilege mode is set to the value encoded in sstatus.SPP.
- The value of sstatus.SPIE is copied into sstatus.SIE.
- The pc is set to the value of sepc.

At this point, control is handed over to software.

6.5 Interrupt Priorities

Individual priorities of global interrupts are determined by the PLIC, as discussed in Chapter 9.

U54-MC Core Complex interrupts are prioritized as follows, in decreasing order of priority:

- Machine external interrupts
- Machine software interrupts
- Machine timer interrupts
- Supervisor external interrupts
- Supervisor software interrupts
- Supervisor timer interrupts

6.6 Interrupt Latency

Interrupt latency for the U54-MC Core Complex is 4 cycles, as counted by the numbers of cycles it takes from signaling of the interrupt to the hart to the first instruction fetch of the handler.

Global interrupts routed through the PLIC incur additional latency of 3 cycles where the PLIC is clocked by clock. This means that the total latency, in cycles, for a global interrupt is: 4 + 3 × (core_clock_0 Hz ÷ clock Hz). This is a best case cycle count and assumes the handler is cached or located in ITIM. It does not take into account additional latency from a peripheral source.

Chapter 7

Bus-Error Unit

This chapter describes the operation of the SiFive Bus-Error Unit.

7.1 Bus-Error Unit Overview

The Bus-Error Unit (BEU) is a per-processor device that records erroneous events and reports them using platform-level and hart-local interrupts. The BEU can be configured to generate interrupts on correctable memory errors, uncorrectable memory errors, and/or TileLink bus errors.

7.2 Reportable Errors

Table 23 lists the events that a Bus-Error Unit may report.

Cause	Meaning
0	*No error*
1	*Reserved*
2	Instruction cache or ITIM correctable ECC error
3	ITIM uncorrectable ECC error
4	*Reserved*
5	Load or store TileLink bus error
6	Data cache correctable ECC error
7	Data cache uncorrectable ECC error

Table 23: `mhpmevent` Register Description

7.3 Functional Behavior

When one of the events listed in Table 23 occurs, the Bus-Error Unit can record information about the event and can generate an interrupt to the PLIC or locally to the hart. The `enable` register contains a mask of which events the BEU can record. Each bit in `enable` corresponds to

an event in Table 23; for example, if `enable`[3] is set, the BEU will record uncorrectable ITIM errors.

The `cause` register indicates the event the BEU has most recently recorded, e.g., a value of 3 indicates an uncorrectable ITIM error. The `cause` value 0 is reserved to indicate no error. `cause` is only written for events enabled in the `enable` register. Furthermore, `cause` is only written when its current value is 0; that is, if multiple events occur, only the first one is latched, until software clears the `cause` register.

The `value` register supplies the physical address that caused the event, or 0 if the address is unknown. The BEU writes the `value` register whenever it writes the `cause` register: i.e., when an event enabled in the `enable` register occurs, and when `cause` contains 0.

The `accrued` register indicates which events have occurred since the last time it was cleared by software. Its format is the same as the `enable` register. The BEU sets bits in the `accrued` register whether or not they are enabled in the `enable` register.

The `plic_interrupt` register indicates which accrued events should generate an interrupt to the PLIC. An interrupt is generated when any bit is set in both `accrued` and `plic_interrupt`, i.e., when (`accrued` & `plic_interrupt`) != 0.

The `local_interrupt` register indicates which accrued events should generate an interrupt directly to the hart associated with this bus-error unit. An interrupt is generated when any bit is set in both `accrued` and `local_interrupt`, i.e., when (`accrued` & `local_interrupt`) != 0}. The interrupt cause is 128; it does not have a bit in the `mie` CSR, so it is always enabled; nor does it have a bit in the `mideleg` CSR, so it cannot be delegated to a mode less privileged than M-mode.

7.4 Memory Map

The Bus-Error Unit memory map is shown in Table 24.

Bus-Error Unit Memory Map				
Offset	**Width**	**Attr.**	**Description**	**Notes**
`0x000`	1B	RW	`cause`	Cause of error event, per Table 23
`0x008`	1B	RW	`value`	Physical address of error event
`0x010`	1B	RW	`enable`	Event enable mask
`0x018`	1B	RW	`plic_interrupt`	Platform-level interrupt-enable mask
`0x020`	1B	RW	`accrued`	Accrued event mask
`0x028`	1B	RW	`local_interrupt`	Hart-local interrupt-enable mask

Table 24: Bus-Error Unit Memory Map

Chapter 8

Core-Local Interruptor (CLINT)

The CLINT block holds memory-mapped control and status registers associated with software and timer interrupts. The U54-MC Core Complex CLINT complies with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*.

8.1 CLINT Memory Map

Table 25 shows the memory map for CLINT on SiFive U54-MC Core Complex.

Address	Width	Attr.	Description	Notes
0x2000000	4B	RW	msip for hart 0	MSIP Registers (1 bit wide)
0x2000004	4B	RW	msip for hart 1	
0x2000008	4B	RW	msip for hart 2	
0x200000c	4B	RW	msip for hart 3	
0x2000010	4B	RW	msip for hart 4	
0x2004028			Reserved	
…				
0x200bff7				
0x2004000	8B	RW	mtimecmp for hart 0	MTIMECMP Registers
0x2004008	8B	RW	mtimecmp for hart 1	
0x2004010	8B	RW	mtimecmp for hart 2	
0x2004018	8B	RW	mtimecmp for hart 3	
0x2004020	8B	RW	mtimecmp for hart 4	
0x2004028			Reserved	
…				
0x200bff7				
0x200bff8	8B	RW	mtime	Timer Register
0x200c000			Reserved	

Table 25: CLINT Register Map

8.2 MSIP Registers

Machine-mode software interrupts are generated by writing to the memory-mapped control register `msip`. Each `msip` register is a 32-bit wide **WARL** register where the upper 31 bits are tied to 0. The least significant bit is reflected in the `MSIP` bit of the `mip` CSR. Other bits in the `msip` registers are hardwired to zero. On reset, each `msip` register is cleared to zero.

Software interrupts are most useful for interprocessor communication in multi-hart systems, as harts may write each other's `msip` bits to effect interprocessor interrupts.

8.3 Timer Registers

`mtime` is a 64-bit read-write register that contains the number of cycles counted from the `rtc_toggle` signal described in the U54-MC Core Complex User Guide. A timer interrupt is pending whenever `mtime` is greater than or equal to the value in the `mtimecmp` register. The timer interrupt is reflected in the `mtip` bit of the `mip` register described in Chapter 6.

On reset, `mtime` is cleared to zero. The `mtimecmp` registers are not reset.

8.4 Supervisor Mode Delegation

By default, all interrupts trap to machine mode, including timer and software interrupts. In order for supervisor timer and software interrupts to trap directly to supervisor mode, supervisor timer and software interrupts must first be delegated to supervisor mode.

Please see Section 6.4 for more details on supervisor mode interrupts.

Chapter 9

Platform-Level Interrupt Controller (PLIC)

This chapter describes the operation of the platform-level interrupt controller (PLIC) on the U54-MC Core Complex. The PLIC complies with *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10* and can support a maximum of 136 external interrupt sources with 7 priority levels.

The U54-MC Core Complex PLIC resides in the `clock` timing domain, allowing for relaxed timing requirements. The latency of global interrupts, as perceived by a hart, increases with the ratio of the `core_clock_0` frequency and the `clock` frequency.

9.1 Memory Map

The memory map for the U54-MC Core Complex PLIC control registers is shown in Table 26. The PLIC memory map has been designed to only require naturally aligned 32-bit memory accesses.

PLIC Register Map				
Address	**Width**	**Attr.**	**Description**	**Notes**
0x0C00_0000			Reserved	
0x0C00_0004	4B	RW	source 1 priority	See Section 9.3 for more information
…				
0x0C00_0220	4B	RW	source 136 priority	
0x0C00_0224			Reserved	
…				
0x0C00_1000	4B	RO	Start of pending array	See Section 9.4 for more information
…				
0x0C00_1010	4B	RO	Last word of pending array	
0x0C00_1014			Reserved	
…				
0x0C00_2000	4B	RW	Start Hart 0 M-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2010	4B	RW	End Hart 0 M-Mode interrupt enables	
0x0C00_2014			Reserved	
…				
0x0C00_2080	4B	RW	Start Hart 1 M-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2090	4B	RW	End Hart 1 M-Mode interrupt enables	
0x0C00_2094			Reserved	
…				
0x0C00_2100	4B	RW	Start Hart 1 S-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2110	4B	RW	End Hart 1 S-Mode interrupt enables	
0x0C00_2114			Reserved	
…				
0x0C00_2180	4B	RW	Start Hart 2 M-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2190	4B	RW	End Hart 2 M-Mode interrupt enables	
0x0C00_2194			Reserved	
…				

Table 26: SiFive PLIC Register Map. Only naturally aligned 32-bit memory accesses are required.

PLIC Register Map				
0x0C00_2200	4B	RW	Start Hart 2 S-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2210	4B	RW	End Hart 2 S-Mode interrupt enables	
0x0C00_2214			Reserved	
…				
0x0C00_2280	4B	RW	Start Hart 3 M-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2290	4B	RW	End Hart 3 M-Mode interrupt enables	
0x0C00_2294			Reserved	
…				
0x0C00_2300	4B	RW	Start Hart 3 S-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2310	4B	RW	End Hart 3 S-Mode interrupt enables	
0x0C00_2314			Reserved	
…				
0x0C00_2380	4B	RW	Start Hart 4 M-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2390	4B	RW	End Hart 4 M-Mode interrupt enables	
0x0C00_2394			Reserved	
…				
0x0C00_2400	4B	RW	Start Hart 4 S-Mode interrupt enables	See Section 9.5 for more information
…				
0x0C00_2410	4B	RW	End Hart 4 S-Mode interrupt enables	
0x0C00_2414			Reserved	
…				
0x0C20_0000	4B	RW	Hart 0 M-Mode priority threshold	See Section 9.6 for more information
0x0C20_0004	4B	RW	Hart 0 M-Mode claim/complete	See Section 9.7 for more information
0x0C20_0008			Reserved	
…				

Table 26: SiFive PLIC Register Map. Only naturally aligned 32-bit memory accesses are required.

PLIC Register Map				
0x0C20_1000	4B	RW	Hart 1 M-Mode priority threshold	See Section 9.6 for more information
0x0C20_1004	4B	RW	Hart 1 M-Mode claim/complete	See Section 9.7 for more information
0x0C20_1008 …			Reserved	
0x0C20_2000	4B	RW	Hart 1 S-Mode priority threshold	See Section 9.6 for more information
0x0C20_2004	4B	RW	Hart 1 S-Mode claim/complete	See Section 9.7 for more information
0x0C20_2008 …			Reserved	
0x0C20_3000	4B	RW	Hart 2 M-Mode priority threshold	See Section 9.6 for more information
0x0C20_3004	4B	RW	Hart 2 M-Mode claim/complete	See Section 9.7 for more information
0x0C20_3008 …			Reserved	
0x0C20_4000	4B	RW	Hart 2 S-Mode priority threshold	See Section 9.6 for more information
0x0C20_4004	4B	RW	Hart 2 S-Mode claim/complete	See Section 9.7 for more information
0x0C20_4008 …			Reserved	
0x0C20_5000	4B	RW	Hart 3 M-Mode priority threshold	See Section 9.6 for more information
0x0C20_5004	4B	RW	Hart 3 M-Mode claim/complete	See Section 9.7 for more information
0x0C20_5008 …			Reserved	
0x0C20_6000	4B	RW	Hart 3 S-Mode priority threshold	See Section 9.6 for more information
0x0C20_6004	4B	RW	Hart 3 S-Mode claim/complete	See Section 9.7 for more information
0x0C20_6008 …			Reserved	
0x0C20_7000	4B	RW	Hart 4 M-Mode priority threshold	See Section 9.6 for more information
0x0C20_7004	4B	RW	Hart 4 M-Mode claim/complete	See Section 9.7 for more information
0x0C20_7008 …			Reserved	

Table 26: SiFive PLIC Register Map. Only naturally aligned 32-bit memory accesses are required.

PLIC Register Map				
0x0C20_8000	4B	RW	Hart 4 S-Mode priority threshold	See Section 9.6 for more information
0x0C20_8004	4B	RW	Hart 4 S-Mode claim/complete	See Section 9.7 for more information
0x0C20_8008			Reserved	
…				
0x1000_0000			End of PLIC Memory Map	

Table 26: SiFive PLIC Register Map. Only naturally aligned 32-bit memory accesses are required.

9.2 Interrupt Sources

The U54-MC Core Complex has 136 interrupt sources. 127 of these are exposed at the top level via the `global_interrupts` signals. Any unused `global_interrupts` inputs should be tied to logic 0. The remainder are driven by various on-chip devices as listed in Table 27. These signals are positive-level triggered.

In the PLIC, as specified in *The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10*, Global Interrupt ID 0 is defined to mean "no interrupt," hence `global_interrupts[0]` corresponds to PLIC Interrupt ID 1.

Source Start	Source End	Source
1	127	External Global Interrupts
128	131	L2 Cache
132	132	Bus Error Unit
133	133	Bus Error Unit
134	134	Bus Error Unit
135	135	Bus Error Unit
136	136	Bus Error Unit

Table 27: PLIC Interrupt Source Mapping

9.3 Interrupt Priorities

Each PLIC interrupt source can be assigned a priority by writing to its 32-bit memory-mapped `priority` register. The U54-MC Core Complex supports 7 levels of priority. A priority value of 0 is reserved to mean "never interrupt" and effectively disables the interrupt. Priority 1 is the lowest active priority, and priority 7 is the highest. Ties between global interrupts of the same priority are broken by the Interrupt ID; interrupts with the lowest ID have the highest effective priority. See Table 28 for the detailed register description.

PLIC Interrupt Priority Register (`priority`)				
Base Address		0x0C00_0000 + 4 × Interrupt ID		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
[2:0]	Priority	RW	X	Sets the priority for a given global interrupt.
[31:3]	Reserved	RO	0	

Table 28: PLIC Interrupt Priority Registers

9.4 Interrupt Pending Bits

The current status of the interrupt source pending bits in the PLIC core can be read from the pending array, organized as 5 words of 32 bits. The pending bit for interrupt ID N is stored in bit $(N \bmod 32)$ of word $(N/32)$. As such, the U54-MC Core Complex has 5 interrupt pending registers. Bit 0 of word 0, which represents the non-existent interrupt source 0, is hardwired to zero.

A pending bit in the PLIC core can be cleared by setting the associated enable bit then performing a claim as described in Section 9.7.

PLIC Interrupt Pending Register 1 (`pending1`)				
Base Address		0x0C00_1000		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	Interrupt 0 Pending	RO	0	Non-existent global interrupt 0 is hard-wired to zero
1	Interrupt 1 Pending	RO	0	Pending bit for global interrupt 1
2	Interrupt 2 Pending	RO	0	Pending bit for global interrupt 2
…				
31	Interrupt 31 Pending	RO	0	Pending bit for global interrupt 31

Table 29: PLIC Interrupt Pending Register 1

PLIC Interrupt Pending Register 5 (`pending5`)				
Base Address		0x0C00_1010		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	Interrupt 128 Pending	RO	0	Pending bit for global interrupt 128
…				
8	Interrupt 136 Pending	RO	0	Pending bit for global interrupt 136
[31:9]	Reserved	WIRI	X	

Table 30: PLIC Interrupt Pending Register 5

9.5 Interrupt Enables

Each global interrupt can be enabled by setting the corresponding bit in the `enables` registers. The `enables` registers are accessed as a contiguous array of 5 × 32-bit words, packed the same way as the `pending` bits. Bit 0 of enable word 0 represents the non-existent interrupt ID 0 and is hardwired to 0.

64-bit and 32-bit word accesses are supported by the `enables` array in SiFive RV64 systems.

PLIC Interrupt Enable Register 1 (`enable1`) for Hart 0 M-Mode				
Base Address		0x0C00_2000		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	Interrupt 0 Enable	RO	0	Non-existent global interrupt 0 is hard-wired to zero
1	Interrupt 1 Enable	RW	X	Enable bit for global interrupt 1
2	Interrupt 2 Enable	RW	X	Enable bit for global interrupt 2
…				
31	Interrupt 31 Enable	RW	X	Enable bit for global interrupt 31

Table 31: PLIC Interrupt Enable Register 1 for Hart 0 M-Mode

PLIC Interrupt Enable Register 5 (`enable5`) for Hart 4 S-Mode				
Base Address		0x0C00_2410		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	Interrupt 128 Enable	RW	X	Enable bit for global interrupt 128
…				
8	Interrupt 136 Enable	RW	X	Enable bit for global interrupt 136
[31:9]	Reserved	RO	0	

Table 32: PLIC Interrupt Enable Register 5 for Hart 4 S-Mode

9.6 Priority Thresholds

The U54-MC Core Complex supports setting of an interrupt priority threshold via the `threshold` register. The `threshold` is a **WARL** field, where the U54-MC Core Complex supports a maximum threshold of 7.

The U54-MC Core Complex masks all PLIC interrupts of a priority less than or equal to `threshold`. For example, a `threshold` value of zero permits all interrupts with non-zero priority, whereas a value of 7 masks all interrupts.

PLIC Interrupt Priority Threshold Register (`threshold`)				
Base Address		0x0C20_0000		
[2:0]	Threshold	RW	X	Sets the priority threshold
[31:3]	Reserved	RO	0	

Table 33: PLIC Interrupt Threshold Register

9.7 Interrupt Claim Process

A U54-MC Core Complex hart can perform an interrupt claim by reading the `claim/complete` register (Table 34), which returns the ID of the highest-priority pending interrupt or zero if there is no pending interrupt. A successful claim also atomically clears the corresponding pending bit on the interrupt source.

A U54-MC Core Complex hart can perform a claim at any time, even if the MEIP bit in its `mip` (Table 11) register is not set.

The claim operation is not affected by the setting of the priority threshold register.

9.8 Interrupt Completion

A U54-MC Core Complex hart signals it has completed executing an interrupt handler by writing the interrupt ID it received from the claim to the `claim/complete` register (Table 34). The PLIC does not check whether the completion ID is the same as the last claim ID for that target. If the completion ID does not match an interrupt source that is currently enabled for the target, the completion is silently ignored.

PLIC Claim/Complete Register (`claim`)				
Base Address		0x0C20_0004		
[31:0]	Interrupt Claim/ Complete for Hart 0 M-Mode	RW	X	A read of zero indicates that no interrupts are pending. A non-zero read contains the id of the highest pending interrupt. A write to this register signals completion of the interrupt id written.

Table 34: PLIC Interrupt Claim/Complete Register for Hart 0 M-Mode

Chapter 10

Error Device

The error device is a TileLink slave that responds to all requests with a TileLink error. It has no registers. The entire memory range discards writes and returns zeros on read. Both operation acknowledgments carry an error indication.

The error device serves a dual role. Internally, it is used as a landing pad for illegal off-chip requests. However, it also useful for testing software handling of bus errors.

Chapter 11

Level 2 Cache Controller

This chapter describes the functionality of the Level 2 Cache Controller used in the U54-MC Core Complex.

11.1 Level 2 Cache Controller Overview

The SiFive Level 2 Cache Controller is used to provide access to fast copies of memory for masters in a Core Complex. The Level 2 Cache Controller also acts as directory-based coherency manager.

The SiFive Level 2 Cache Controller offers extensive flexibility as it allows for several features in addition to the Level 2 Cache functionality. These include memory-mapped access to L2 Cache RAM for disabled cache ways, scratchpad functionality, way masking and locking, ECC support with error tracking statistics, error injection, and interrupt signaling capabilities.

These features are described in Section 11.2.

11.2 Functional Description

The U54-MC Core Complex L2 Cache Controller is configured into 1 banks. Each bank contains 512 sets of 8 ways and each way contains a 64-byte block. This subdivision into banks helps facilitate increased available bandwidth between CPU masters and the L2 Cache as each bank has its own dedicated TL-C inner port. As such, multiple requests to different banks may proceed in parallel.

The outer Memory port(s) of the L2 Cache Controller is shared among all banks and typically connected to cacheable memory. The overall organization of the L2 Cache Controller is depicted in Figure 3. See the U54-MC Core Complex User Guide for detailed information regarding the Memory port.

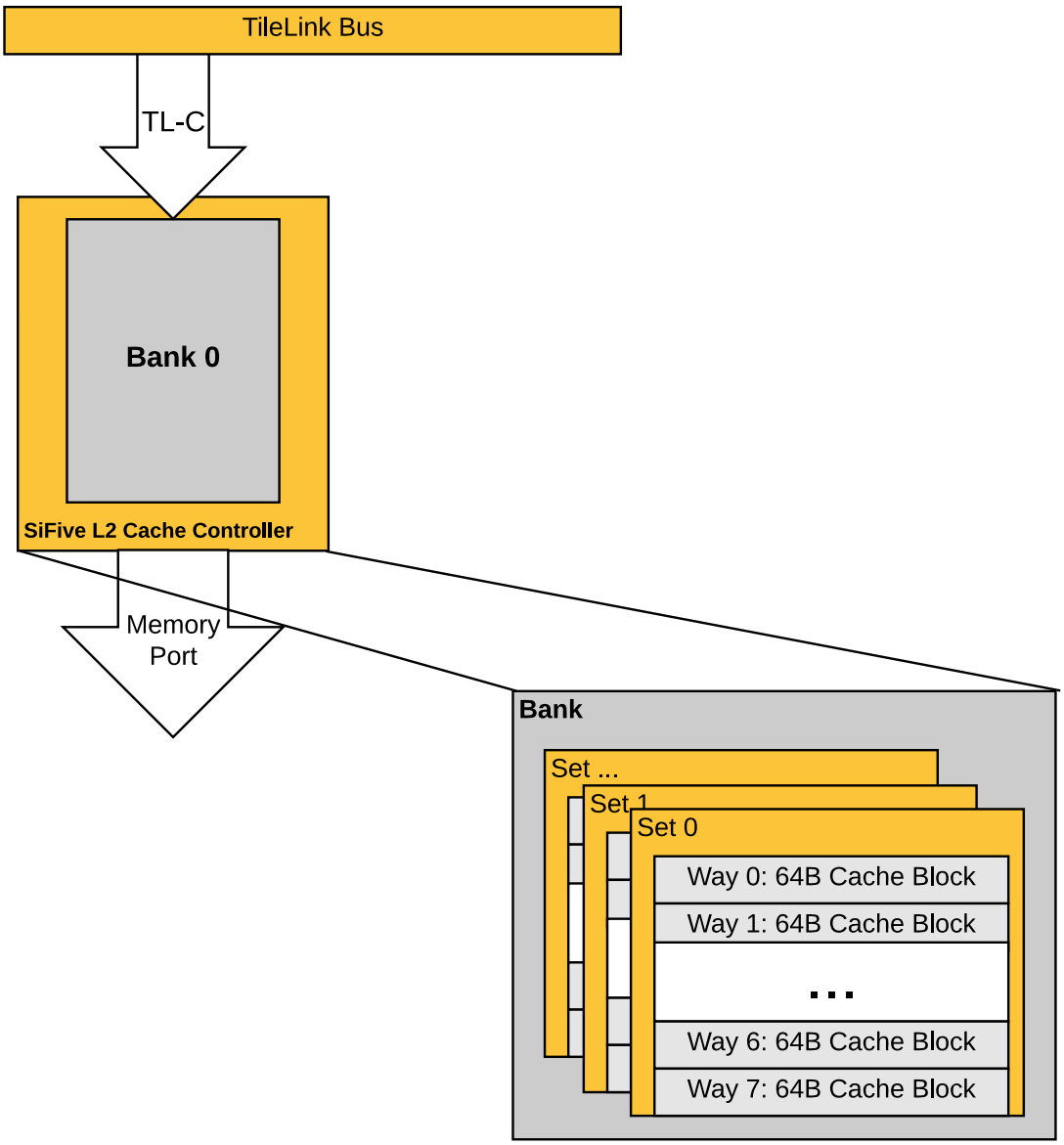

Figure 3: Organization of the SiFive L2 Cache Controller

11.2.1 Way Enable and the L2 Loosely Integrated Memory (L2-LIM)

Similar to the ITIM discussed in Chapter 3, the SiFive Level 2 Cache Controller allows for its SRAMs to act either as direct addressed memory in the Core Complex address space or as a cache that is controlled by the L2 Cache Controller and which can contain a copy of any cacheable address.

When cache ways are disabled, they are addressable in the L2 Loosely Integrated Memory (L2-LIM) address space as described in the U54-MC Core Complex memory map in Chapter 5. Fetching instructions or data from the L2-LIM provides deterministic behavior equivalent to an

L2 cache hit, with no possibility of a cache miss. Accesses to L2-LIM are always given priority over cache way accesses, which target the same L2 cache bank.

Out of reset, all ways, except for way 0, are disabled. Cache ways can be enabled by writing to the `WayEnable` register described in Section 11.4.2. Once a cache way is enabled, it can not be disabled unless the U54-MC Core Complex is reset. The highest numbered L2 Cache Way is mapped to the lowest L2-LIM address space, and way 1 occupies the highest L2-LIM address range. As L2 cache ways are enabled, the size of the L2-LIM address space shrinks. The mapping of L2 cache ways to L2-LIM address space is show in Figure 4.

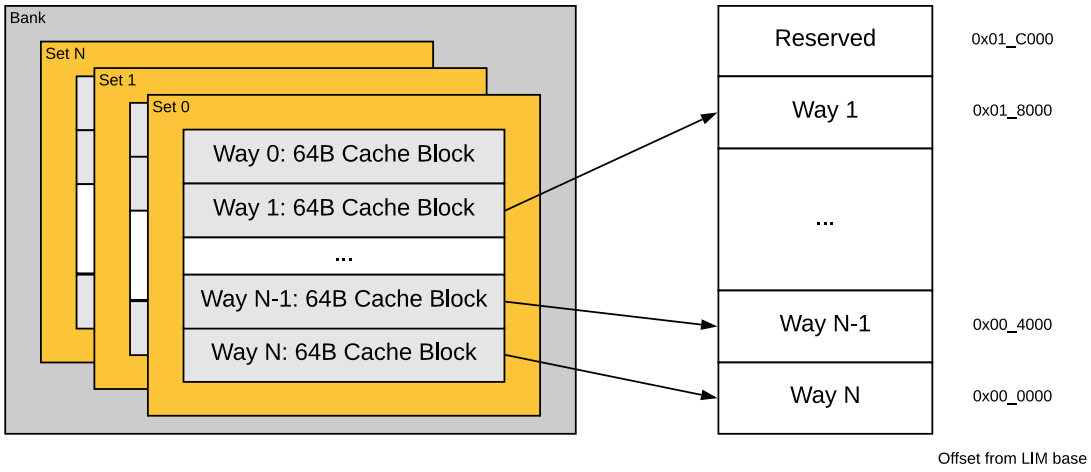

Figure 4: Mapping of L2 Cache Ways to L2-LIM Addresses

11.2.2 Way Masking and Locking

The SiFive L2 Cache Controller can control the amount of cache memory a CPU master is able to allocate into by using the `WayMaskX` register described in Section 11.4.12. Note that `WayMaskX` registers only affect allocations, and reads can still occur to ways that are masked. As such, it becomes possible to lock down specific cache ways by masking them in all `WayMaskX` registers. In this scenario, all masters can still read data in the locked cache ways but cannot evict data.

11.2.3 L2 Scratchpad

The SiFive L2 Cache Controller has a dedicated scratchpad address region that allows for allocation into the cache using an address range which is not memory backed. This address region is denoted as the L2 Zero Device in the Memory Map in Chapter 5. Writes to the scratchpad region allocate into cache ways that are enabled and not masked. Care must be taken with the scratchpad, however, as there is no memory backing this address space. Cache evictions from addresses in the scratchpad result in data loss.

The main advantage of the L2 Scratchpad over the L2-LIM is that it is a cacheable region allowing for data stored to the scratchpad to also be cached in a master's L1 data cache resulting in faster access.

The recommended procedure for using the L2 Scratchpad is as follows:

1. Use the `WayEnable` register to enable the desired cache ways.
2. Designate a single master that will allocate into the scratchpad. For this procedure, we designate this master as Master S. All other masters (CPU and non-CPU) are denoted as Masters X.
3. Masters X: Write to the `WayMaskX` register to mask the ways that are to be used for the scratchpad. This prevents Masters X from evicting cache lines in the designated scratchpad ways.
4. Master S: Write to the `WayMaskX` register to mask all ways *except* the ways that are to be used for the scratchpad. At this point, Master S should only be able to allocate into the cache ways meant to be used as a scratchpad.
5. Master S: Write scratchpad data into the L2 Scratchpad address range (L2 Zero Device).
6. Master S: Repeat steps 4 and 5 for each way to be used as scratchpad.
7. Master S: Use the `WayMaskX` register to mask the scratchpad ways for Master S so that it is no longer able to evict cache lines from the designated scratchpad ways.
8. At this point, the scratchpad ways should contain the scratchpad data, with all masters able to read, write, and execute from this address space, and no masters able to evict the scratchpad contents.

11.2.4 Error Correcting Codes (ECC)

The SiFive Level 2 Cache Controller supports ECC. ECC is applied to both categories of SRAM used, the data SRAMs and the meta-data SRAMs (index, tag, and directory information). The data SRAMs use Single Error Correction and Double Error Detection (SECDED). The meta-data SRAMs use Single Error Correction (SEC).

Whenever a correctable error is detected, the cache immediately repairs the corrupted bit and writes it back to SRAM. This corrective procedure is completely invisible to application software. However, to support diagnostics, the cache records the address of the most recently corrected meta-data and data errors. Whenever a new error is corrected, a counter is increased and an interrupt is raised. There are independent addresses, counters, and interrupts for correctable meta-data and data errors.

`DirFail`, `DirError`, `DataError`, and `DataFail` signals are used to indicate that an L2 meta-data, data, or uncorrectable L2 data error has occurred, respectively. These signals are connected to the PLIC as described in Chapter 9 and are cleared upon reading their respective count registers.

11.3 Memory Map

The L2 Cache Controller memory map is shown in Table 35.

Offset	Name	Description
0x000	Config	Information about the Cache Configuration
0x008	WayEnable	The index of the largest way which has been enabled. May only be increased.
0x040	ECCInjectError	Inject an ECC Error
0x100	DirECCFixLow	The low 32-bits of the most recent address to fail ECC
0x104	DirECCFixHigh	The high 32-bits of the most recent address to fail ECC
0x108	DirECCFixCount	Reports the number of times an ECC error occured
0x140	DatECCFixLow	The low 32-bits of the most recent address to fail ECC
0x144	DatECCFixHigh	The high 32-bits of the most recent address to fail ECC
0x148	DatECCFixCount	Reports the number of times an ECC error occured
0x160	DatECCFailLow	The low 32-bits of the most recent address to fail ECC
0x164	DatECCFailHigh	The high 32-bits of the most recent address to fail ECC
0x168	DatECCFailCount	Reports the number of times an ECC error occured
0x200	Flush64	Flush the phsyical address equal to the 64-bit written data from the cache
0x240	Flush32	Flush the physical address equal to the 32-bit written data << 4 from the cache
0x800	WayMask0	Master 0 way mask register
0x808	WayMask1	Master 1 way mask register
0x810	WayMask2	Master 2 way mask register
0x818	WayMask3	Master 3 way mask register
0x820	WayMask4	Master 4 way mask register
0x828	WayMask5	Master 5 way mask register
0x830	WayMask6	Master 6 way mask register
0x838	WayMask7	Master 7 way mask register
0x840	WayMask8	Master 8 way mask register
0x848	WayMask9	Master 9 way mask register
0x850	WayMask10	Master 10 way mask register
0x858	WayMask11	Master 11 way mask register
0x860	WayMask12	Master 12 way mask register
0x868	WayMask13	Master 13 way mask register
0x870	WayMask14	Master 14 way mask register
0x878	WayMask15	Master 15 way mask register
0x880	WayMask16	Master 16 way mask register
0x888	WayMask17	Master 17 way mask register
0x890	WayMask18	Master 18 way mask register
0x898	WayMask19	Master 19 way mask register
0x8A0	WayMask20	Master 20 way mask register

Table 35: Register offsets within the L2 Cache Controller Control Memory Map

11.4 Register Descriptions

This section describes the functionality of the memory-mapped registers in the Level 2 Cache Controller.

11.4.1 Cache Configuration Register (Config)

The Config Register can be used to programmatically determine information regarding the cache size and organization.

Config: Information about the Cache Configuration (Config)				
Register Offset		0x0		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
[7:0]	Banks	RO	0x4	Number of banks in the cache
[15:8]	Ways	RO	0x10	Number of ways per bank
[23:16]	lgSets	RO	0x9	Base-2 logarithm of the sets per bank
[31:24]	lgBlockBytes	RO	0x6	Base-2 logarithm of the bytes per cache block

Table 36: Config: Information about the Cache Configuration

11.4.2 Way Enable Register (WayEnable)

The WayEnable register determines which ways of the Level 2 Cache Controller are enabled as cache. Cache ways that are not enabled are mapped into the U54-MC Core Complex's L2-LIM (Loosely Integrated Memory) as described in the memory map in Chapter 5.

This register is initialized to 0 on reset and may only be increased. This means that, out of reset, only a single L2 cache way is enabled, as one cache way must always remain enabled. Once a cache way is enabled, the only way to map it back into the L2-LIM address space is by a reset.

WayEnable: The index of the largest way which has been enabled. May only be increased. (WayEnable)				
Register Offset		0x8		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
[7:0]	WayEnable	RW	0x0	The index of the largest way which has been enabled. May only be increased.
[31:8]	Reserved			

Table 37: WayEnable: The index of the largest way which has been enabled. May only be increased.

11.4.3 ECC Error Injection Register (ECCInjectError)

The ECCInjectError register can be used to insert an ECC error into either the backing data or meta-data SRAM. This function can be used to test error correction logic, measurement, and recovery.

ECCInjectError: Inject an ECC Error (ECCInjectError)				
Register Offset		0x40		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
[7:0]	ECCToggleBit	RW	0x0	Toggle (corrupt) this bit index on the next cache operation
[15:8]	Reserved			
16	ECCToggleType	RW	0x0	Toggle (corrupt) a bit in 0=data or 1=directory
[31:17]	Reserved			

Table 38: ECCInjectError: Inject an ECC Error

11.4.4 ECC Directory Fix Address (DirECCFix*)

The DirECCFixHi and DirECCFixLow registers are read-only registers that contain the address of the most recently corrected meta-data error. This field supplies only the portions of the address that correspond to the affected set and bank, since all ways are corrected together.

11.4.5 ECC Directory Fix Count (DirECCFixCount)

The DirECCFixCount register is a read-only register that contains the number of corrected L2 meta-data errors.

Reading this register clears the DirError interrupt signal described in Section 11.2.4.

11.4.6 ECC Directory Fail Address (DirECCFail*)

The DirECCFailLow and DirECCFailHigh registers are read-only registers that contains the address of the most recent uncorrected L2 meta-data error.

11.4.7 ECC Data Fix Address (DatECCFix*)

The DatECCFixLow and DatECCFixHigh registers are read-only registers that contain the address of the most recently corrected L2 data error.

11.4.8 ECC Data Fix Count (DatECCFixCount)

The DataECCFixCount register is a read-only register that contains the number of corrected data errors.

Reading this register clears the DataError interrupt signal described in Section 11.2.4.

11.4.9 ECC Data Fail Address (DatECCFail*)

The DatECCFailLow and DatECCFailHigh registers are a read-only registers that contain the address of the most recent uncorrected L2 data error.

11.4.10 ECC Data Fail Count (`DatECCFailCount`)

The `DatECCFailCount` register is a read-only register that contains the number of uncorrected data errors.

Reading this register clears the `DataFail` interrupt signal described in Section 11.2.4.

11.4.11 Cache Flush Registers (`Flush*`)

The U54-MC Core Complex L2 Cache Controller provides two registers that can be used for flushing specific cache blocks.

`Flush64` is a 64-bit write-only register that flushes the cache block containing the address written. `Flush32` is a 32-bit write-only register that flushes a cache block containing the written address left shifted by 4 bytes. In both registers, all bits must be written in a single access for the flush to take effect.

11.4.12 Way Mask Registers (`WayMask*`)

The `WayMaskX` register allows a master connected to the L2 Cache Controller to specify which L2 cache ways can be evicted by master `X`. Masters can still access memory cached in masked ways. The mapping between masters and their L2 master IDs is shown in Table 41.

At least one cache way must be enabled. It is recommended to set/clear bits in this register using atomic operations.

WayMask0: Master 0 way mask register (`WayMask0`)				
Register Offset		`0x800`		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	`WayMask0[0]`	`RW`	`0x1`	Enable way 0 for Master 0
1	`WayMask0[1]`	`RW`	`0x1`	Enable way 1 for Master 0
2	`WayMask0[2]`	`RW`	`0x1`	Enable way 2 for Master 0
3	`WayMask0[3]`	`RW`	`0x1`	Enable way 3 for Master 0
4	`WayMask0[4]`	`RW`	`0x1`	Enable way 4 for Master 0
5	`WayMask0[5]`	`RW`	`0x1`	Enable way 5 for Master 0
6	`WayMask0[6]`	`RW`	`0x1`	Enable way 6 for Master 0
7	`WayMask0[7]`	`RW`	`0x1`	Enable way 7 for Master 0
8	`WayMask0[8]`	`RW`	`0x1`	Enable way 8 for Master 0
9	`WayMask0[9]`	`RW`	`0x1`	Enable way 9 for Master 0
10	`WayMask0[10]`	`RW`	`0x1`	Enable way 10 for Master 0
11	`WayMask0[11]`	`RW`	`0x1`	Enable way 11 for Master 0
12	`WayMask0[12]`	`RW`	`0x1`	Enable way 12 for Master 0
13	`WayMask0[13]`	`RW`	`0x1`	Enable way 13 for Master 0
14	`WayMask0[14]`	`RW`	`0x1`	Enable way 14 for Master 0
15	`WayMask0[15]`	`RW`	`0x1`	Enable way 15 for Master 0
[63:16]	Reserved			

Table 39: WayMask0: Master 0 way mask register

…

WayMask20: Master 20 way mask register (`WayMask20`)				
Register Offset		`0x8A0`		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	`WayMask20[0]`	`RW`	`0x1`	Enable way 0 for Master 20
1	`WayMask20[1]`	`RW`	`0x1`	Enable way 1 for Master 20
2	`WayMask20[2]`	`RW`	`0x1`	Enable way 2 for Master 20
3	`WayMask20[3]`	`RW`	`0x1`	Enable way 3 for Master 20
4	`WayMask20[4]`	`RW`	`0x1`	Enable way 4 for Master 20
5	`WayMask20[5]`	`RW`	`0x1`	Enable way 5 for Master 20
6	`WayMask20[6]`	`RW`	`0x1`	Enable way 6 for Master 20
7	`WayMask20[7]`	`RW`	`0x1`	Enable way 7 for Master 20
8	`WayMask20[8]`	`RW`	`0x1`	Enable way 8 for Master 20
9	`WayMask20[9]`	`RW`	`0x1`	Enable way 9 for Master 20
10	`WayMask20[10]`	`RW`	`0x1`	Enable way 10 for Master 20
11	`WayMask20[11]`	`RW`	`0x1`	Enable way 11 for Master 20
12	`WayMask20[12]`	`RW`	`0x1`	Enable way 12 for Master 20
13	`WayMask20[13]`	`RW`	`0x1`	Enable way 13 for Master 20
14	`WayMask20[14]`	`RW`	`0x1`	Enable way 14 for Master 20
15	`WayMask20[15]`	`RW`	`0x1`	Enable way 15 for Master 20
[63:16]	Reserved			

Table 40: WayMask20: Master 20 way mask register

Master ID	Description
0	Core 0 D-Cache MMIO
1	Core 0 I-Cache
2	Core 1 D-Cache
3	Core 1 I-Cache
4	Core 2 D-Cache
5	Core 2 I-Cache
6	Core 3 D-Cache
7	Core 3 I-Cache
8	Core 4 D-Cache
9	Core 4 I-Cache
10	AXI4 front port ID #0
11	AXI4 front port ID #1
12	AXI4 front port ID #1
13	AXI4 front port ID #3

Table 41: Master IDs in the L2 Cache Controller

Chapter 12

Debug

This chapter describes the operation of SiFive debug hardware, which follows *The RISC-V Debug Specification 0.13*. Currently only interactive debug and hardware breakpoints are supported.

12.1 Debug CSRs

This section describes the per-hart trace and debug registers (TDRs), which are mapped into the CSR space as follows:

CSR Name	Description	Allowed Access Modes
`tselect`	Trace and debug register select	D, M
`tdata1`	First field of selected TDR	D, M
`tdata2`	Second field of selected TDR	D, M
`tdata3`	Third field of selected TDR	D, M
`dcsr`	Debug control and status register	D
`dpc`	Debug PC	D
`dscratch`	Debug scratch register	D

Table 42: Debug Control and Status Registers

The `dcsr`, `dpc`, and `dscratch` registers are only accessible in debug mode, while the `tselect` and `tdata1-3` registers are accessible from either debug mode or machine mode.

12.1.1 Trace and Debug Register Select (`tselect`)

To support a large and variable number of TDRs for tracing and breakpoints, they are accessed through one level of indirection where the `tselect` register selects which bank of three `tdata1-3` registers are accessed via the other three addresses.

The `tselect` register has the format shown below:

Trace and Debug Select Register			
CSR	`tselect`		
Bits	**Field Name**	**Attr.**	**Description**
[31:0]	index	WARL	Selection index of trace and debug registers

Table 43: `tselect` CSR

The `index` field is a **WARL** field that does not hold indices of unimplemented TDRs. Even if `index` can hold a TDR index, it does not guarantee the TDR exists. The `type` field of `tdata1` must be inspected to determine whether the TDR exists.

12.1.2 Trace and Debug Data Registers (`tdata1-3`)

The `tdata1-3` registers are XLEN-bit read/write registers selected from a larger underlying bank of TDR registers by the `tselect` register.

Trace and Debug Data Register 1			
CSR	`tdata1`		
Bits	**Field Name**	**Attr.**	**Description**
[27:0]	TDR-Specific Data		
[31:28]	type	RO	Type of the trace & debug register selected by `tselect`

Table 44: `tdata1` CSR

Trace and Debug Data Registers 2 and 3			
CSR	`tdata2/3`		
Bits	**Field Name**	**Attr.**	**Description**
[31:0]	TDR-Specific Data		

Table 45: `tdata2/3` CSRs

The high nibble of `tdata1` contains a 4-bit `type` code that is used to identify the type of TDR selected by `tselect`. The currently defined `types` are shown below:

Type	Description
0	No such TDR register
1	Reserved
2	Address/Data Match Trigger
≥ 3	Reserved

Table 46: `tdata` Types

The `dmode` bit selects between debug mode (`dmode`=1) and machine mode (`dmode`=1) views of the registers, where only debug mode code can access the debug mode view of the TDRs. Any

attempt to read/write the `tdata1-3` registers in machine mode when `dmode`=1 raises an illegal instruction exception.

12.1.3 Debug Control and Status Register (`dcsr`)

This register gives information about debug capabilities and status. Its detailed functionality is described in *The RISC-V Debug Specification 0.13*.

12.1.4 Debug PC `dpc`

When entering debug mode, the current PC is copied here. When leaving debug mode, execution resumes at this PC.

12.1.5 Debug Scratch `dscratch`

This register is generally reserved for use by Debug ROM in order to save registers needed by the code in Debug ROM. The debugger may use it as described in *The RISC-V Debug Specification 0.13*.

12.2 Breakpoints

The U54-MC Core Complex supports two hardware breakpoint registers per hart, which can be flexibly shared between debug mode and machine mode.

When a breakpoint register is selected with `tselect`, the other CSRs access the following information for the selected breakpoint:

CSR Name	Breakpoint Alias	Description
`tselect`	`tselect`	Breakpoint selection index
`tdata1`	`mcontrol`	Breakpoint match control
`tdata2`	`maddress`	Breakpoint match address
`tdata3`	N/A	Reserved

Table 47: TDR CSRs when used as Breakpoints

12.2.1 Breakpoint Match Control Register `mcontrol`

Each breakpoint control register is a read/write register laid out in Table 48.

Breakpoint Control Register (`mcontrol`)				
Register Offset		CSR		
Bits	**Field Name**	**Attr.**	**Rst.**	**Description**
0	R	WARL	X	Address match on LOAD
1	W	WARL	X	Address match on STORE
2	X	WARL	X	Address match on Instruction FETCH
3	U	WARL	X	Address match on User Mode
4	S	WARL	X	Address match on Supervisor Mode
5	Reserved	WPRI	X	Reserved
6	M	WARL	X	Address match on Machine Mode
[10:7]	match	WARL	X	Breakpoint Address Match type
11	chain	WARL	0	Chain adjacent conditions.
[17:12]	action	WARL	0	Breakpoint action to take. 0 or 1.
18	timing	WARL	0	Timing of the breakpoint. Always 0.
19	select	WARL	0	Perform match on address or data. Always 0.
20	Reserved	WPRI	X	Reserved
[26:21]	maskmax	RO	4	Largest supported NAPOT range
27	dmode	RW	0	Debug-Only access mode
[31:28]	type	RO	2	Address/Data match type, always 2

Table 48: Test and Debug Data Register 3

The `type` field is a 4-bit read-only field holding the value 2 to indicate this is a breakpoint containing address match logic.

The `bpaction` field is an 8-bit read-write **WARL** field that specifies the available actions when the address match is successful. The value 0 generates a breakpoint exception. The value 1 enters debug mode. Other actions are not implemented.

The R/W/X bits are individual **WARL** fields, and if set, indicate an address match should only be successful for loads/stores/instruction fetches, respectively, and all combinations of implemented bits must be supported.

The M/S/U bits are individual **WARL** fields, and if set, indicate that an address match should only be successful in the machine/supervisor/user modes, respectively, and all combinations of implemented bits must be supported.

The `match` field is a 4-bit read-write **WARL** field that encodes the type of address range for breakpoint address matching. Three different `match` settings are currently supported: exact, NAPOT, and arbitrary range. A single breakpoint register supports both exact address matches and matches with address ranges that are naturally aligned powers-of-two (NAPOT) in size. Breakpoint registers can be paired to specify arbitrary exact ranges, with the lower-numbered breakpoint register giving the byte address at the bottom of the range and the higher-numbered

breakpoint register giving the address 1 byte above the breakpoint range, and using the `chain` bit to indicate both must match for the action to be taken.

NAPOT ranges make use of low-order bits of the associated breakpoint address register to encode the size of the range as follows:

`maddress`	Match type and size
`a…aaaaaa`	Exact 1 byte
`a…aaaaa0`	2-byte NAPOT range
`a…aaaa01`	4-byte NAPOT range
`a…aaa011`	8-byte NAPOT range
`a…aa0111`	16-byte NAPOT range
`a…a01111`	32-byte NAPOT range
…	…
`a01…1111`	2^{31}-byte NAPOT range

Table 49: NAPOT Size Encoding

The `maskmax` field is a 6-bit read-only field that specifies the largest supported NAPOT range. The value is the logarithm base 2 of the number of bytes in the largest supported NAPOT range. A value of 0 indicates that only exact address matches are supported (1-byte range). A value of 31 corresponds to the maximum NAPOT range, which is 2^{31} bytes in size. The largest range is encoded in `maddress` with the 30 least-significant bits set to 1, bit 30 set to 0, and bit 31 holding the only address bit considered in the address comparison.

To provide breakpoints on an exact range, two neighboring breakpoints can be combined with the `chain` bit. The first breakpoint can be set to match on an address using `action` of 2 (greater than or equal). The second breakpoint can be set to match on address using `action of 3` (less than). Setting the `chain` bit on the first breakpoint prevents the second breakpoint from firing unless they both match.

12.2.2 Breakpoint Match Address Register (`maddress`)

Each breakpoint match address register is an XLEN-bit read/write register used to hold significant address bits for address matching and also the unary-encoded address masking information for NAPOT ranges.

12.2.3 Breakpoint Execution

Breakpoint traps are taken precisely. Implementations that emulate misaligned accesses in software will generate a breakpoint trap when either half of the emulated access falls within the address range. Implementations that support misaligned accesses in hardware must trap if any byte of an access falls within the matching range.

Debug-mode breakpoint traps jump to the debug trap vector without altering machine-mode registers.

Machine-mode breakpoint traps jump to the exception vector with "Breakpoint" set in the `mcause` register and with `badaddr` holding the instruction or data address that caused the trap.

12.2.4 Sharing Breakpoints Between Debug and Machine Mode

When debug mode uses a breakpoint register, it is no longer visible to machine mode (that is, the `tdrtype` will be 0). Typically, a debugger will leave the breakpoints alone until it needs them, either because a user explicitly requested one or because the user is debugging code in ROM.

12.3 Debug Memory Map

This section describes the debug module's memory map when accessed via the regular system interconnect. The debug module is only accessible to debug code running in debug mode on a hart (or via a debug transport module).

12.3.1 Debug RAM and Program Buffer (`0x300–0x3FF`)

The U54-MC Core Complex has 16 32-bit words of program buffer for the debugger to direct a hart to execute arbitrary RISC-V code. Its location in memory can be determined by executing `aiupc` instructions and storing the result into the program buffer.

The U54-MC Core Complex has two 32-bit words of debug data RAM. Its location can be determined by reading the `DMHARTINFO` register as described in the RISC-V Debug Specification. This RAM space is used to pass data for the Access Register abstract command described in the RISC-V Debug Specification. The U54-MC Core Complex supports only general-purpose register access when harts are halted. All other commands must be implemented by executing from the debug program buffer.

In the U54-MC Core Complex, both the program buffer and debug data RAM are general-purpose RAM and are mapped contiguously in the Core Complex memory space. Therefore, additional data can be passed in the program buffer, and additional instructions can be stored in the debug data RAM.

Debuggers must not execute program buffer programs that access any debug module memory except defined program buffer and debug data addresses.

The U54-MC Core Complex does not implement the `DMSTATUS.anyhavereset` or `DMSTATUS.allhavereset` bits.

12.3.2 Debug ROM (`0x800–0xFFF`)

This ROM region holds the debug routines on SiFive systems. The actual total size may vary between implementations.

12.3.3 Debug Flags (`0x100–0x110`, `0x400–0x7FF`)

The flag registers in the debug module are used for the debug module to communicate with each hart. These flags are set and read used by the debug ROM and should not be accessed by any program buffer code. The specific behavior of the flags is not further documented here.

12.3.4 Safe Zero Address

In the U54-MC Core Complex, the debug module contains the address `0x0` in the memory map. Reads to this address always return 0, and writes to this address have no impact. This property allows a "safe" location for unprogrammed parts, as the default `mtvec` location is `0x0`.

Chapter 13

References

Visit the SiFive forums for support and answers to frequently asked questions: https://forums.sifive.com

[1] A. Waterman and K. Asanovic, Eds., The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.2, May 2017. [Online]. Available: https://riscv.org/specifications/

[2] ——, The RISC-V Instruction Set Manual Volume II: Privileged Architecture Version 1.10, May 2017. [Online]. Available: https://riscv.org/specifications/