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Errata Classification

The document lists all of the known issues impacting the FU740-C000 as of February 5, 2021.

The following table describes each errata category severity level (i.e. "CAT" level):

<table>
<thead>
<tr>
<th>CAT-A</th>
<th>A critical error with high probability &amp; the absence of an effective workaround.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAT-B</td>
<td>A significant error with high/medium probability and an acceptable workaround, or a minor error with a high probability (regardless of workaround), or a critical error with medium/low probability.</td>
</tr>
<tr>
<td>CAT-C</td>
<td>A minor error with high/medium probability or significant error with low probability and an acceptable workaround.</td>
</tr>
</tbody>
</table>

The errata category classification is derived from the following impact/probability relationship:

<table>
<thead>
<tr>
<th>Probability of an errata to manifest</th>
<th>Impact</th>
<th>Minor (feature limiting)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>CAT-A</td>
<td>CAT-B</td>
</tr>
<tr>
<td>Medium</td>
<td>CAT-B</td>
<td>CAT-B</td>
</tr>
<tr>
<td>Low</td>
<td>CAT-B</td>
<td>CAT-C</td>
</tr>
<tr>
<td></td>
<td>CAT-C</td>
<td>CAT-C</td>
</tr>
</tbody>
</table>
CIP-231

Title
7-Series Fetch PC out of reset can be incorrect

Implication
The fetch PC can depend on the I-Cache RAM contents at reset, but only matters for the first instruction out of reset. This depends on the random contents of the I-Cache and only is observable for rare values.

One place this is especially noticeable is being able to debug from the first instruction out of reset as the correct $PC value may not be reported in $DPC.

Workaround
None

Impact
Medium

Probability
Low

Category
CAT-C
CIP-253

Title
DRET does not raise illegal instruction when executed out of debug mode.

Implication
The RISC-V Debug Specifications states that DRET should result in an illegal instruction exception when executed outside of debug mode. When this erratum is present, in M-mode a DRET instruction does not cause an illegal instruction exception.

Workaround
None

Impact
Minor

Probability
Low

Category
CAT-C
CIP-286

Title
Debug Module/ROM Accessible in M-Mode

Implication
It is possible to access Debug Module memory region in M-Mode, whereas the Debug Specification indicates that region should only be accessible in Debug Mode.

Workaround
Do not access Debug Module memory region from M-Mode.

Impact
Minor

Probability
Low

Category
CAT-C
CIP-403

Title
Debug.SBCS has incorrect reset value for SBACCESS

Implication
The RISC-V Debug Specification and SiFive documentation both say that the Debug.SBCS.SBACCESS reset value should be 2. It is actually 0.

Workaround
Set Debug.SBCS.SBACCESS to the desired value before performing any SBA operations.

Impact
Minor

Probability
High

Category
CAT-B
Title
Debug SBA: some sbaccess sizes are not checked for legality

Implication
An access error should be flagged but is not. The operation will result in possible memory corruption near the SBA access address during a write transaction or invalid data returned for a read transaction.

Workaround
Ensure sbaccess is set to a legal value (0-4) before starting an SBA transaction.

Impact
Medium

Probability
Low

Category
CAT-C
CIP-453

Title
stval/mtval CSRs are not sign-extended for instruction access/page fault exceptions

Implication
In normal use, negative addresses are used by the kernel, and the kernel doesn't page out its code pages. Therefore, an instruction page fault manifesting this bug is not expected to occur; and if it does occur, the kernel should treat it as a fatal error anyway. If the kernel tried to use stval to handle the page fault, then it would incorrectly see an invalid address rather than a valid one.

Workaround
If instruction page faults with negative addresses do not need to be resumable, as is the case for Linux, no workaround is necessary.

In other cases, the correct value for mtval can be computed with the expression \((\text{mepc} + \text{mepc} \text{^} \text{mtval}) \text{ & 2}\). This expression only holds for instruction page faults and access exceptions. For other exceptions, use the value from mtval directly.

The same workarounds apply to stval, replacing mepc with sepc.

Impact
Minor

Probability
Low

Category
CAT-C
CIP-473

Title
In Timer/WDT/PWM Peripheral, some bits are read in the wrong fields

Implication
It is not possible to read the current value of the deglitch bit in the Timer peripheral. Instead, the value of the zerocmp bit is reported instead in the deglitch bit offset. The zerocmp offset is undefined.

Workaround
Adjust software that wants to read the zerocmp bit to read the deglitch offset.

Do not rely on the value in the zerocmp offset.

Impact
Minor

Probability
High

Category
CAT-B
CIP-546

Title
When performance counters are set to count exceptions, they do not count other retirement events

Implication
It is not possible to use the same performance counter to count both exceptions and other retirement events (including instructions retired of specific type). Doing so will lead to incorrect counts for the other events.

Workaround
Use two separate counters: one for exception events and one for other instructions of interest.

Impact
Minor

Probability
Medium

Category
CAT-B
CIP-575

Title
L2 Sideband can report ECC error even after it was overwritten

Implication
The L2 Sideband includes a path to bypass data from older writes to newer hazardous requests, but still uses the corrected/uncorrected ECC result from the over-written entry for several cycles.

Workaround
Delay subsequent reads until the write has finished, such as by writing multiple times (3 times is sufficient).

Impact
Medium

Probability
Low

Category
CAT-C
CIP-576

Title
L2 response can report ECC error even after being overwritten

Implication
The L2 D-Channel response includes a path to bypass data from older writes to newer hazardous requests, but still uses the result of the ECC check (i.e., ECC_correct/corrected_ECC_error/uncorrected_ECC_error) from the over-written entry for several cycles. This means that there is a short window of time during which an ECC error may be reported even once it has been overwritten.

Workaround
Tolerate multiple ECC errors reported for a single cache entry.

Impact
Minor

Probability
Low

Category
CAT-C
CIP-582

Title
L2: Response can fail to report an ECC error if the data is read immediately after a corrupt write-back from the L1.

Implication
The L2 D-Channel response includes a path to bypass data from older writes to newer hazardous requests, but still uses the result of the ECC check (ie, ECC_correct/corrected_ECC_error/uncorrected_ECC_error) from the over-written entry for several cycles. This means that an ECC error may not cause a Bus Error Unit interrupt if an entry is read via a sub-cacheline sized read (eg a read from a core without an L1 DCache) within a few cycles of a cacheline write which is marked as corrupt.

For our designs, this situation will only be encountered when an L1 DCache line is evicted to the L2 Cache and an uncorrectable error is detected in that L1 line.

NOTE: In this scenario, the error will be detected during the eviction process. However, another core may read the data without the error being reported on that read.

Workaround
Detect all L1 ECC errors for all cores and use that as notification for uncorrectable errors.

Impact
Minor

Probability
Low

Category
CAT-C
CIP-589

Title
L2 Sideband can report no ECC error if read immediately after corrupt data is written

Implication
The L2 Sideband includes a path to bypass data from older writes to newer hazardous requests, but still uses the corrected/uncorrected ECC result from the over-written entry for several cycles.

Workaround
Delay subsequent reads until the write has finished, such as by writing multiple times (3 times is sufficient).

Impact
Medium

Probability
Low

Category
CAT-C
CIP-595

Title
Disabling the Debug Module during an SBA transaction can cause TileLink network hang.

Implication
If a debugger sets dmactive to 0 while there is an SBA transaction in progress, the Debug Module will drop d.ready and could cause the transaction to hang, which could cause the entire internal network to hang and the core will not make forward progress.

Workaround
The debugger should ensure there is no SBA transaction in progress before setting dmactive to 0.

Impact
Medium

Probability
Low

Category
CAT-C
CIP-737

Title
mcause values does not reset to 0 after reset

Implication
mcause cannot be used to determine the cause of reset.

Workaround
Do not rely on the mcause value to determine reset condition; however, always assume that SiFive implementations do not distinguish different reset conditions.

Impact
Minor

Probability
High

Category
CAT-B
CIP-818

Title
Potential bus hang when flushing L2 or L3 Cache

Implication
A flush command sent to the MMIO control port of the ComposableCache (L2/L3) can cause the ComposableCache to fail to release an MSHR. This can eventually lead to the bus hanging.

Workaround
None

Impact
Critical

Probability
Low

Category
CAT-B
CIP-899

Title
ECC error in D$ can cause store to be dropped

Implication
In a situation consisting of a store to address A, load from some address, store to address A, then load, the second store can be dropped if there is a correctable/uncorrectable ECC error detected.

The second store to address A does not take effect, but the error is still reported to the Bus Error Unit.

Since the bug can only manifest with two nearby stores to the same word, the first not detecting an error and the second detecting an error, this bug is not likely to occur in practice. In particular, if the error formed before the sequence began, the bug would not manifest.

Workaround
None at this time

Impact
Medium

Probability
Low

Category
CAT-B
CIP-930

Title
Race condition between write to *status.FS and floating point load that changes *status.FS.

Implication
This errata occurs when a floating-point load is issued, then software clears mstatus.FS (setting it to 0x0, OFF), then the load writeback occurs. The load writeback can erroneously set the mstatus.FS to DIRTY, resulting in mstatus.FS being DIRTY instead of OFF at the completion of the instruction sequence.

This sequence of events can only occur for MMIO floating point loads.

Workaround
Execute a fence before setting mstatus.FS = OFF (0x0).

Impact
Minor

Probability
Low

Category
CAT-C
CIP-951

Title
   Pseudo-Least-Recently-Used (PLRU) algorithm does not fully utilize non-power-of-2 cache ways or TLB Entries

Implication
   Slight performance degradation — some ways of the cache or TLB will never be evicted

Workaround
   None needed, minor performance impact.

Impact
   Minor

Probability
   High

Category
   CAT-B
CIP-993

Title
MTVAL/STVAL CSR set to incorrect value following EBREAK instruction

Implication
MTVAL/STVAL should be 0 following an EBREAK instruction; instead, it is set to an arbitrary value.

Workaround
Do not rely on the value of MTVAL/STVAL following an EBREAK instruction. EBREAK being the cause of an exception can be identified by examining MCAUSE (for M-mode) or SCAUSE (for S-mode).

Impact
Minor

Probability
Medium

Category
CAT-C
Title
Core livelocks as it keeps getting an I$ miss

Implication
The Core livelocks as an instruction cache miss will be continuously suppressed if the Instruction Cache thinks the access is speculative and tries to fetch from non-cacheable memory.

Workaround
None at this time

Impact
Critical

Probability
Medium

Category
CAT-B
CIP-1200

Title
Instruction TLB can fail to respect a non-global SFENCE

Implication
If an SFENCE.VMA with rs1 != x0 or rs2 != x0 happens on the same cycle as an I-TLB refill, the refill still occurs, even if the SFENCE.VMA should've flushed the entry being refilled.

This can lead to stale page mappings marked as valid in the TLB, which can in-turn allow unprivileged accesses, a security hole.

A global sfence.vma must be issued to properly invalidate TLB entries, which would have only performance implications and not functional.

Workaround
Flush the TLB using SFENCE.VMA x0, x0

Impact
Critical

Probability
Low

Category
CAT-B
CIP-1246

Title
Illegal addresses are not always detected in Debug SBA

Implication
SBA may generate read transactions to illegal memory addresses when sbreadondata is set and sbdata0 is read. These illegal addresses normally alias to some other address in the system but generally have no other effect. OpenOCD starts a block read with sbreadonaddress and continues with sbreadondata so this bug only appears if a block read starts at a legal address and extends into an illegal range.

Workaround
Use sbreadonaddress to generate read transactions based on writes to sbaddress0. These are properly checked for legality.

Impact
Minor

Probability
Low

Category
CAT-C
CIP-1293

Title
An L2TLB write will almost always block the next L2TLB search, even many cycles later.

Implication
Performance impact only. In almost all cases, the Core would behave as if it doesn't have an L2 TLB.

Workaround
Set bit 0 ("Disable data cache clock gating") of the Feature Disable CSR (0x7c1) to disable D-Cache clock gating.

Impact
Medium

Probability
High

Category
CAT-B
CIP-1464

Title
Chained triggers with both instruction and data never fire

Implication
Hardware allows 2 triggers to be chained, meaning both conditions must be satisfied at the same time for the trigger to fire. When a chain includes both instruction trigger and data address trigger, the breakpoint does not fire.

Workaround
Set a data trigger on any access to the data item, then in the GDB breakpoint command script, check whether the PC is the one you want and restart if not.

Impact
Minor

Probability
High

Category
CAT-B