Embedding Intelligence Everywhere with SiFive 7 Series Core IP

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Embedded Intelligence Everywhere

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Intelligence Migrating to the Edge
On-Device Embedded Intelligence quickly Gaining momentum
RISC-V ISA is Ideal for Domain Specific Architecture

- Legacy ISA’s Are Decades Old
- RISC-V Unlocks the Architecture & Enables Innovation
- RISC-V ISA is Open Source

Simple, Stable, Clean Slate Design, Modular, Designed for Extendibility/Specialization

Designed for Extendibility/Specialization
SiFive Core IP
Embedding Intelligence Everywhere

**Consumer**
AR/VR/Gaming devices
Smart Home
Imaging/Wearables

**Storage/Networking/5G**
SSD, SAN, NAS
Base Stations, Small cells, APs
Switches, Smart NICs, Offload cards

**ML/Edge**
Sensor Hubs, Gateways
Autonomous machines
IoT devices
AR/VR/Sensor Fusion

- **Low Latency peripheral access** and coherent accelerator port
- **Coherent in-cluster combination** of application processors with real-time processors
- **Simple caching hierarchy** for ease of application optimization
- **Combine** with SiFive 2, 3 or 5 series for designs with tight power constraints
- **Workload specific customizations** (AR/VR/MR/CV)
- **Mixed precision arithmetic** for accelerating machine learning compute
### Storage

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coherent in-cluster combination</td>
<td>of application processors and real-time processors</td>
</tr>
<tr>
<td>Configurable memory maps and coherent accelerator ports</td>
<td>for tightly coupling storage specific accelerators</td>
</tr>
<tr>
<td>Deterministic mode</td>
<td>for FAST DATA applications with hard real-time constraints</td>
</tr>
<tr>
<td>Tightly integrated memories and Cache lock capability</td>
<td>for critical real time workloads</td>
</tr>
<tr>
<td>Optional FPU</td>
<td>for applications which don’t need floating point capability</td>
</tr>
<tr>
<td>Storage, ML, Cryptography specific custom instructions</td>
<td></td>
</tr>
<tr>
<td>64-bit real-time addressability</td>
<td>for BIG DATA applications</td>
</tr>
</tbody>
</table>
5G/Networking

- **Complex arithmetic** capability for accelerating baseband functions
- **In-cluster coherence of application and real-time processor** enables 5G latency (<1ms) requirements
- **High bandwidth accelerator ports** for enabling intelligent offload processing
- **Hard real-time capabilities** for scheduling baseband protocol layers
- **Configurable memory maps** for optimizing QoS
- **High throughput** processing for next gen 5G stacks
- **Tightly Integrated Memories and Cache lock capability** for critical real time workloads
SiFive Core IP

U Cores
64-bit Application Processors

S Cores
64-bit Embedded Processors

E Cores
32-bit Embedded Processors

Embedding Intelligence from the Edge to the Cloud

Intelligent Cloud

Intelligent Edge
SiFive Core IP
2 series:

SiFive’s **smallest** and most **efficient** RISC-V processor IP
SiFive Core IP 3 and 5 series:

The world's most deployed RISC-V processor IP

- Efficient Performance
  - Coherent, Heterogenous, Multicore
  - Hard Real-time capabilities
- Configurable
- Efficient
- Mature

32-bit Embedded Processors
64-bit Embedded Processors
64-bit Application Processors
SiFive Core IP 7 series:

The highest performance in-order commercial RISC-V processor IP

**E7 Series**
- 32-bit Embedded Processors

**S7 Series**
- 64-bit Embedded Processors

**U7 Series**
- 64-bit Application Processors

Common Feature sets
- Hard Real-time capabilities
- Unprecedented scalability

- High Performance
- Multicore Scalability
- Rich Configurable Feature Set
SiFive Core IP
8 series:

Most scalable Out-of-order RISC-V processor IP

Unprecedented scalability
Optimized for highest perf/watt

64-bit Application Processors

2x Area Efficiency*

1.5x Power Efficiency*

Richer Feature Set*

*Compared to Equivalent Competing Cores
SiFive Core IP 150+ Design Wins!

- Efficient Performance
- Scalability
- Compelling Feature Set

Embedding intelligence for a world of a Trillion Connected Devices
Rapid adoption of SiFive Core IP from the Edge to the Core
Silicon verified. Market proven.

The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

- Microcontrollers
- Embedded
- Linux
- Multicore
- Networking
- Storage
- Computing
- AI
- Industrial
- IoT
- Consumer
- Automotive

www.sifive.com
SiFive 7 series Core IP

Jahoor Vohra
Director, FAE
SiFive, Inc.
SiFive Core IP
7 series:

The highest performance in-order commercial RISC-V processor IP
SiFive 7 Series
Embedded Intelligence Everywhere

Scalable throughput provided by 8+1 cores per cluster

Extensible design via custom instructions

Configurable memory architecture for application specific tuning

Tightly integrated memory for low latency access

64-bit addressability for real-time latency sensitive applications

Mixed-precision arithmetic for efficient compute of ML workloads

Enhanced determinism for hard real-time constraints

Functional safety provided by in-built fault tolerance mechanisms

A single pre-integrated and verified deliverable

Cache lock capability for mission-critical computing

In-cluster coherent combination of real-time and application processors
Linley MPR – “SiFive Raises RISC-V Performance”

SiFive Raises RISC-V Performance
Series 7 Comprises First Superscalar RISC-V CPUs

By Bob Wheeler (November 12, 2018)

Designing a CPU that scales from microcontrollers to server-class processors in RISC-V is difficult. But SiFive’s approach with its 7-series line is the Linley Hill Processors Conference, the RISC-V showing it had its first CPU. The die-in-order design is the most complex so far, moving into the same class as Arm’s “Gold” Cortex-A family. SiFive will offer versions of this real-time embedded processor as well as Linux applications.

At the high end, the company’s new U760H industrial-grade (125°C) core builds on the U70, which already offers multimedia configurations and Linux compatibility. The standard U760H includes a single-precision floating-point unit (FPU). It supports a wide range of instructions, including SIMD instructions. The standard U760H includes a single-precision floating-point unit (FPU). It supports a wide range of instructions, including SIMD instructions.

Rocket Percentage
The new, dual-issue 7-series CPU represents a departure from SiFive’s previous designs, which are based on the open-source RISC-V core. The U760H offers a single-threaded scalable pipeline that scales 32GB in TSMC 28nm technology (4GHz FPU@9GHz). The RISC-V U760H has 32-bit RISC-V, which implements the RISC-V ISA (like UltraSparc U70). It is the first processor to include a multiply and divide unit (MAD), and can perform 16-bit, 32-bit, and 64-bit operations. Optionally, it handles single-precision (FP) and double-precision (DP) floating-point instructions. SiFive is developing a microcontroller for Internet 7-series cores, but the RISC-V vector (V) extensions remain incomplete. The U760H supports all integer and simple integer operations, including multiplication, division, and floating-point operations. It also supports vector operations and integer operations (including multiplication, integer division, and floating-point operations). SiFive added a second 64-bit mode and a second memory access stage to add a large 16-byte cache and write-back capabilities. A second double-precision floating-point unit (FP) enables double-precision operations and reduces the latency to the next instruction.

Rocket Pipeline
The Rocket 7-series pipeline, with its multi-stage, 16-stage decode and 24-stage execute stages, enables larger TMs without reducing clock speeds.

Table 1. SiFive-versus-Arm CPU comparison

<table>
<thead>
<tr>
<th></th>
<th>SiFive E76</th>
<th>Arm Cortex-M7</th>
<th>SiFive U74</th>
<th>Arm Cortex-A55</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Set</td>
<td>32-bit RISC-V</td>
<td>32-bit Arm v7-M</td>
<td>64-bit RISC-V</td>
<td>64-bit Arm v8</td>
</tr>
<tr>
<td>Max Clock Freq</td>
<td>1.6GHz→</td>
<td>1.1GHz→</td>
<td>1.6GHz→</td>
<td>1.6GHz→</td>
</tr>
<tr>
<td>Max IPC</td>
<td>2 IPC</td>
<td>2 IPC</td>
<td>2 IPC</td>
<td>2 IPC</td>
</tr>
<tr>
<td>CoreMark Perf</td>
<td>4.9CM/MHz</td>
<td>5.0CM/MHz</td>
<td>4.9CM/MHz</td>
<td>4.4CM/MHz</td>
</tr>
<tr>
<td>Die Area*</td>
<td>0.065mm²</td>
<td>0.067mm²</td>
<td>0.22mm²</td>
<td>0.65mm²</td>
</tr>
</tbody>
</table>

source: https://www.linleygroup.com/mpr (12 Nov 2018)
7 Series Microarchitecture Overview
E7 Series Features

- E7 core architectural features
  - RV32GCV capable core
  - Dual Issue, in-order 8-stage Harvard Pipeline
- Very flexible memory system
  - Optional I$ and D$
  - Optional I and D TIM interfaces
  - Optional Fast IO Port (FIO) per core
- Multi-core capable with coherency and optional L2
- Deterministic fast interrupt responses
- Higher throughput and efficiency vs Cortex-M7
  - 2.3 DMIPS/MHz
  - 4.9 CoreMarks/MHz
S7 Series
Features

- S7 core architectural features
  - RV64GCV capable core
  - Dual Issue, in-order 8-stage Harvard Pipeline
- Very flexible memory system
  - Optional I$ and D$
  - Optional I and D TIM interfaces
  - Optional Fast IO Port (FIO) per core
- Multi-core capable with coherency and optional L2
- Deterministic fast interrupt responses
- Higher throughput and efficiency vs Cortex-R8
  - 2.5 DMIPS/MHz
  - 4.9 CoreMarks/MHz
U7 Series Features

- **U7 Core Architectural Features**
  - RV64GCV capable core
  - Sv39 Virtual Memory Support
  - Dual Issue, in-order 8 stage Harvard Pipeline

- **Heterogenous in-cluster combination of applications processor and real-time processor supported**

- **Configurable Level 2 Cache with cache lock capability and Tightly Integrated Memory available**

- **Functional Safety and Security and Real Time features**
  - SECDED ECC on all L1 and L2 memories
  - PMP and MMU for memory protection
  - **Programmatically clear and/or disable dynamic branch prediction** for deterministic execution and enhanced security

- **Extremely competitive performance vs Cortex-A55 with higher efficiency and throughput**
  - 2.5 DMIPS/MHz
  - 4.9 CoreMarks/MHz
7 Series Pipeline
E7/S7 Level 1 Memory System

Meets High-Performance and Deterministic Application requirements

- Optional Instruction Cache
- Data Cache or Data Tightly Integrated Memory (DTIM)
- Optional Instruction Tightly Integrated Memory (ITIM)
- Optional, configurable, Fast IO Port

Dotted lines represent optional interfaces/modules
## E7/S7 Series Improvements

<table>
<thead>
<tr>
<th></th>
<th>E3/S5 Series</th>
<th>E7/S7 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pipeline</td>
<td>In-order, 5-7 stage pipeline</td>
<td>In-order, 8 stage pipeline</td>
</tr>
<tr>
<td>ISA</td>
<td>RV32IMAFDC/RV64IMAFDC</td>
<td>RV32IMAFDCV/RV64IMAFDCV</td>
</tr>
<tr>
<td>Floating Point</td>
<td>Optional (F or D)</td>
<td>Optional (F or D)</td>
</tr>
<tr>
<td>Issue Width</td>
<td>Single-issue</td>
<td>Dual-Issue</td>
</tr>
<tr>
<td>Instruction Subsystem</td>
<td>Instruction Cache with reconfigurable ITIM</td>
<td>Optional Instruction Cache and Optional ITIM</td>
</tr>
<tr>
<td>Data Subsystem</td>
<td>Data Cache or DTIM</td>
<td>Data Cache or DTIM + FIO SRAM</td>
</tr>
<tr>
<td>Load to Use Delay</td>
<td>1 Cycle</td>
<td>0 Cycle</td>
</tr>
<tr>
<td>SRAM access time</td>
<td>5 + N cycles</td>
<td>2 + N cycles (FIO SRAM) worst case</td>
</tr>
<tr>
<td>(SRAM has N cycles latency)</td>
<td></td>
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</tbody>
</table>
SiFive Insight - Debug and Trace Solution

Access, Observe, Control

SiFive’s Insight gives developers the power to efficiently debug SiFive based designs. From simple run control debug, to cross-triggering, to advanced multicore trace solutions, all delivered pre-integrated and verified together with SiFive’s RISC-V Core IP in a single deliverable.

SiFive Insight Debug and Trace IP
Enabling secure debug, Nexus trace, advanced debug control, and Arm® CoreSight™ compatibility.
SiFive Shield

A Scalable, Complete, Platform Security Solution

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<tr>
<th>Root of Trust</th>
<th>Threat Prevention</th>
<th>Verified Crypto</th>
<th>Software</th>
<th>Communications</th>
<th>Secure Lifecycle</th>
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<tr>
<td>Formally Verified</td>
<td>SiFive WorldGuard</td>
<td>FOSS Crypto Library</td>
<td>FOSS WorldGuard Monitor</td>
<td>Cloud Service Provider Connector</td>
<td>Formal Verifications</td>
</tr>
<tr>
<td>Secure Debug</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FOSS Secure Update</td>
<td></td>
<td>RSA/ECDSA</td>
<td>Linux</td>
<td>s2n TLS</td>
<td></td>
</tr>
<tr>
<td>FOSS Secure Boot/uBoot</td>
<td></td>
<td>SHA</td>
<td>FreeRTOS</td>
<td>s2n TLS Wrapper</td>
<td>Secure Supply Chain</td>
</tr>
<tr>
<td>Key Provisioning</td>
<td></td>
<td>AES</td>
<td>OpenSSL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Key Storage</td>
<td></td>
<td>TRNG</td>
<td>Freedom SDK</td>
<td>s2n SSL Wrapper</td>
<td></td>
</tr>
<tr>
<td>Unique S/N</td>
<td></td>
<td></td>
<td>Freedom Metal BSP</td>
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</tr>
</tbody>
</table>

RISC-V PMP/PMA

SiFive Core IP

RISC-V ISA

SiFive

RISC-V Foundation

Community or 3rd party

External Lab Security Evaluation

Community Security Evaluation
- ITIM and FIO Ports provide fast local SRAM and Accelerators
  - Also globally addressable
- Coherent System with a shared Level 2 Cache Controller
  - Shared, Cacheable, Coherent SRAM for fast performance with bounded latencies
- Front Port allows other masters access to U7-MC Core Complex Memories
  - Can also signal MSIs to CLICs
Core IP 7 Series
Standard Cores

01  E76, E76-MC
02  S76, S76-MC
03  U74, U74-MC

"Standard Cores represent pre-configured implementations of a Core Series which are available for free RTL and FPGA evaluations."
Customize your Cores

- **SiFive Core Designer** enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal

- **Variants** are generated with click of a button and are available from the Workspace

- **Variants** contain
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal **BSP** for easy integration into SiFive’s SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC
SiFive Core IP 7 Series

- Efficient Performance
- Scalability
- Compelling Feature Set

Embedding intelligence for a world of a Trillion Connected Devices